

# Radiation Imaging Detectors Made by Wafer Post-processing of CMOS Chips

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# Radiation Imaging Detectors Made by Wafer Post-processing of CMOS Chips

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# Chapter 1

## Introduction

This thesis shows how microtechnology fabrication techniques can be used to fabricate fully integrated gaseous radiation imaging detectors. Using these fabrication techniques radiation detectors were built on top of CMOS<sup>1</sup> chips.

This introduction chapter presents the concepts of wafer post-processing and Micro Patterned Gaseous Detectors (MPGDs), both of which underpin much of what follows in the subsequent chapters.

### 1.1 Wafer post-processing

The semiconductor industry has developed fast since the invention of the transistor in 1947 [1] and the integrated circuit in 1959 [2]. In his famous 1965 paper [3], Gordon E. Moore proposed the number of components in an integrated circuit will double roughly every year; and today microchips can contain over one billion transistors [4]. A vast amount of fabrication skills have been accumulated when trying to reduce size and improve reliability and yield. But CMOS technology is not only used to build integrated circuits that store and process information. It can be applied to fabricate a wide variety of other sensing and actuating structures. Typical examples are MEMS<sup>2</sup> and lab-on-a-chip devices [5], [6].

CMOS chips and sensing devices are interconnected to obtain on-device circuitry. In a classic approach, CMOS chips and sensors/actuators are built in

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<sup>1</sup>Complementary Metal Oxide Semiconductor.

<sup>2</sup>Microelectromechanical systems

separate lines. Later on, they are assembled together and electrically interconnected. A more attractive approach is the integration of sensing part and CMOS chip in a single device. This way several benefits can be obtained. As the signal is directly picked up the origin the device would have higher sensitivity, lower power consumption and can perform at higher speed. Also the size and mass of the final device is reduced. A price reduction is expected when produced in large quantities.

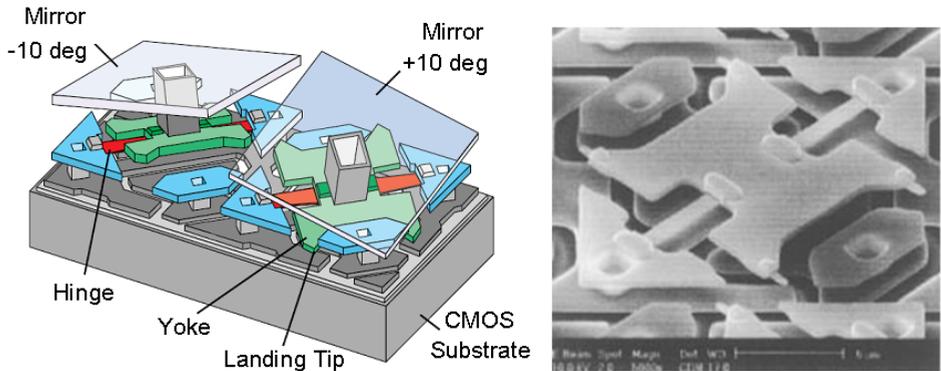
The sensor/actuator device can be added at several stages of the CMOS fabrication process [7], [8]:

- Before the CMOS fabrication starts.
- In an intermediate CMOS fabrication step. The CMOS processing is stopped to add intermediate layers.
- After the CMOS process has been completed.

In the latter case two fabrication options are viable. The sensor can be obtained by micromachining of the different metal and insulator layers already present in the chip [9]. In the second option the structure is built on top of the CMOS, leaving untouched the chip [10], [11], [12]. Figure 1.1 shows a paradigmatic example of this approach; the so called digital micromirrors [13]. An aluminum mirror structure is built on top of a CMOS chip. The mirrors can be positioned at two different angle states. Depending of the angle, incident light is projected into or out of the pupil lens. The angle the mirrors are tilted is controlled by the microchip beneath. These micromirrors are commercially used in image projection systems.

The post-processing steps should not affect the performance of the integrated circuit. Some cautions must be taken during the manufacturing of the sensing part on the CMOS chips [14]:

- Wafer temperature should not exceed 400 °C - 450 °C.
- Plasmas should be used carefully due to the risk of plasma charging damage.
- The thickness and type of materials must be chosen not to introduce excessive mechanical stress.
- The hydrogen passivation of the transistors must be maintained.
- Chemical contamination, that occupies deep level interstitials in silicon, should be avoided.



**Figure 1.1:** Schematic view of two digital micromirrors positioned at different states (left). SEM picture of yoke and hinges of a micromirror (right) [13].

In this work, several wafer post-processing steps are applied to CMOS chips in order to fabricate radiation imaging devices. With this approach the performance of previously manually assembled detectors is enhanced.

## 1.2 Micro patterned gaseous detectors

Until 1970 ionizing radiation tracking was performed with devices read out with a camera. Pictures of the track were taken. Typical examples are the nuclear film emulsion, spark chamber or the bubble chamber. The bubble chamber provides good spatial resolution. It needs a relatively long recovery time after an event. For the bubble chamber operation a big vessel is filled with a liquid close to its boiling point. Ionizing radiation passing through the liquid volume leaves a track of bubbles. Pictures of the inside of the chamber were taken. Tracks are later analyzed off-line.

In 1968 the wire chamber [15] was introduced by Charpak and coworkers. It represented the starting point to the electronic read out of the track left by electrically charged particles traversing a gas volume. A series of wires are stretched in between two cathode planes. The system is mounted inside a chamber filled with gas. High voltage is applied to the cathode planes and the anode wires. When a particle passes the gas volume it ionizes the medium and produces electrons that drift toward the wires. A signal is induced in some wires. The signal's location

and time information can be used to reconstruct the particle trajectory.

The invention of the Micro Strip Gas Counter (MSGC) by A. Oed [16] introduced a new generation of detectors; generally named as Micropatterned Gaseous Detectors. Oed substituted the wires of the wire chamber by alternated anode and cathode metal strips on a glass substrate. MPGDs benefits include the following:

- Very good control of the dimensions.
- High counting rate can be achieved.
- High granularity.

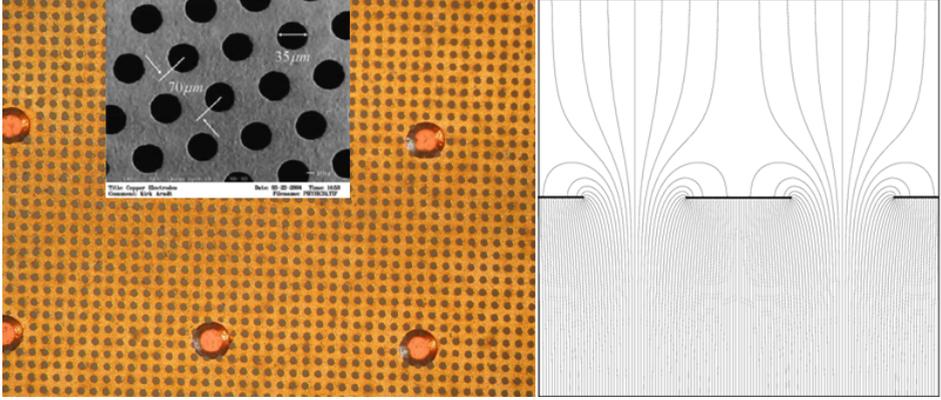
Since the invention of the MSGC many other Micropatterned Gaseous Detectors have been produced. The most popular, GEM [17] and Micromegas [18], are commonly used in nuclear and high energy physics.

### 1.2.1 The Micro Mesh Gaseous detector

The Micro Mesh Gaseous Detector (Micromegas) was invented by Giomataris *et al.* in 1995. It employs a punctured metal foil ( $\sim 5 \mu\text{m}$  thick). Holes in the foil have around  $35 \mu\text{m}$  diameter and  $60 \mu\text{m}$  pitch. The foil is suspended over an anode plane by means of insulating pillars ( $50 \mu\text{m}$  to  $100 \mu\text{m}$  tall). Figure 1.2 (left) shows an optical microscope and detailed scanning electron microscope (SEM) image of a Micromegas foil.

The foil separates the drift region, where the primary charge is produced, from the amplification region. When ionizing radiation (e.g., a cosmic ray particle or an X-ray) crosses the gas volume above the grid, electrons are liberated and driven towards the anode by a moderate electric field ( $\sim 1 \text{ kV/cm}$ ). A high electric field ( $\sim 80 \text{ kV/cm}$ ) is applied between the grid and the anode. Each free electron will create an ionization avalanche in this region; yielding an exponential increase in the number of free electrons. The avalanche electrons are collected at the anode. Figure 1.2 (right) shows the electric field configuration in the amplification region produced by a Micromegas foil.

Micromegas presents a reduced dependence of the gain on small gap variations, on pressure changes or on temperature fluctuations [19] and a very homogeneous electric field. Thanks to this property a very good energy resolution can be obtained (11.8% full width half maximum (FWHM) at 5.9 keV X-rays [20]). Micromegas offers an excellent spatial resolution (finally defined by the mesh hole pitch). A spatial resolution of  $14 \mu\text{m}$  has been previously shown [21]. Spatial resolutions of  $35 \mu\text{m}$  and  $30 \mu\text{m}$  are reported for MWPC and MSGC respectively [22], [23].

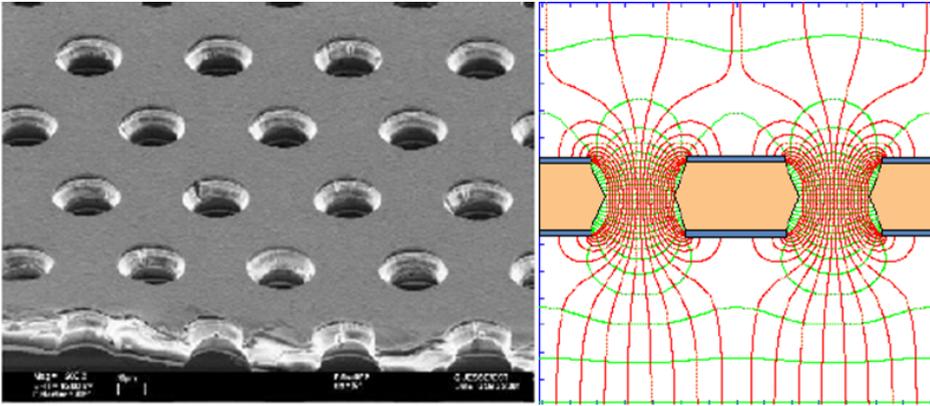


**Figure 1.2:** Left: Optical microscope image of a Micromegas foil and SEM image (inset) of a Micromegas foil of Purdue University/3M (G. Bolla and I. Shipsey). Right: Typical electric field shape in the amplification region of a Micromegas.

### 1.2.2 The Gas Electron Multiplier

The Gas Electron Multiplier (GEM) was introduced by Sauli's group at CERN in 1996. It consists of an insulating foil, metallised on both sides. Typically a kapton foil  $50 \mu\text{m}$  thick is used as insulator although thicker GEMs are available [24]. Holes are made in the foil with about  $70 \mu\text{m}$  diameter and  $140 \mu\text{m}$  pitch. Figure 1.3 (left) shows a SEM picture of a GEM foil.

The GEM foil is stretched in a frame and suspended some millimeters over the anode plane. A electric field of about  $50 \text{ kV/cm}$  is applied between the GEM electrodes. Electrons created in the region above the GEM are driven toward the GEM holes by a moderate drift field. The high electric field across the GEM makes that every free electron entering a hole will create an ionization avalanche. Thus the number of electrons increases exponentially. Charge is extracted from the GEM by a weak transfer field and collected at the anode. Figure 1.3 (right) shows the electric field close to the GEM foil. The focusing and defocusing of the electric field lines is clearly seen. Two or three GEMs are usually assembled in cascade to achieve the required gain and to lower the spark risk [25].

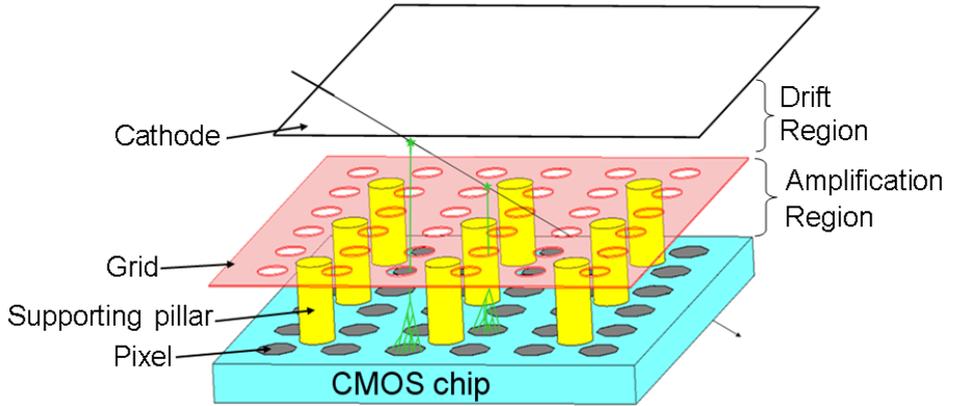


**Figure 1.3:** Left: SEM image of a GEM foil built at CERN (image from CERN GDD group). Right: Typical electric field shape in the amplification region of a GEM (image from CERN TS-DEM group).

### 1.2.3 Electronic readout of MPGD's

For both GEM and Micromegas, typically, a charge-sensitive amplifier is used to record arrival time, position, and pulse height of the avalanche electrons collected at the anode. The combination of MPGD and amplifier forms a radiation detector that is relatively cheap and of low mass, and consumes little power. It finds application in nuclear, high energy, and astrophysics, as well as biology, medicine, and industrial radiology [26].

When a microchip is used as the anode every hole has its own channel [27], [28] and the signal is directly picked up at the origin (schematic in figure 1.4). This reduces the capacitance of the sensing electrode, leading to noise reduction. Therefore very high sensitivity can be reached. Single electron detection at a gain of few thousands is possible. The microchip typically has an array of bond pads (for picking up the charge) each connected to a preamplifier and buffer. With a manually mounted grid, misalignment between the holes in the grid and pixels on the chip leads to Moiré effects [29]. Inactive pixel areas are produced during assembling. High volume production would be laborious. To overcome these, fabrication of the grid by means of CMOS wafer post-processing is pursued. This is assumed to lead to a better detector performance at a lower cost.



**Figure 1.4:** Schematic view of the detector. An ionizing particle creates several free electrons that drift toward the CMOS chip and create an avalanche between the grid and the chip.

### 1.3 Outline of the thesis

In this thesis, wafer post-processing technology is developed and used to fabricate radiation detectors on top of CMOS chips. These detectors are intended for charged high-energy particle tracking applications.

In chapter 2 we explain the fabrication process used to build the detectors on CMOS chips. Two different types of devices, InGrid and GEMGrid were produced by wafer scale and chip scale post-processing.

Chapter 3 is devoted to the impact of the geometry of the detector on the gain and energy resolution. This study was done on dummy silicon wafers with an aluminized anode. This study was a prerequisite before integrating the device on a CMOS chip.

Chapter 4 deals with the protection of Micropatterned Gaseous Detectors against sparks. Different materials were tested to protect the microchip against the lethal discharges.

In chapter 5 we present a comparative analysis between InGrid and GEMGrid devices showing their breakdown voltage behavior and tracking capabilities.

New multilayer structures fabricated by stacking an InGrid device on top of another InGrid or GEMGrid structure are introduced in chapter 6. First results on the operation of these detectors are presented.

In chapter 7 we analyze the reliability of our detectors. We found that two of the main sources that can degrade detectors behavior are moisture exposure and mechanical attacks. The impact of these hazards is quantified in a series of experiments. Solutions against these hazards are presented.

Final conclusions and future recommendations are given in chapter 8.

# Chapter 2

## Wafer post-processing for MPGD's

This chapter treats the fabrication of Micro Patterned Gaseous Detectors using MEMS techniques compatible with CMOS post-processing.

Micromegas-like and GEM-like structures built on top of readout chips are introduced. Wafer level post-processing and single chip post-processing have been performed successfully. Different metals and deposition techniques were investigated for the mesh electrode.

### 2.1 Introduction

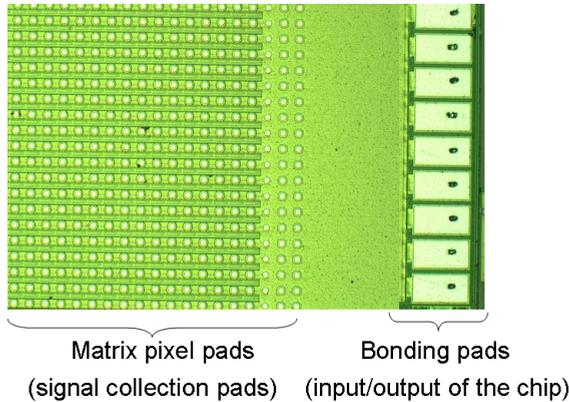
In the following sections we will describe how Micromegas-like structures, named InGrid (INtegrated Grid) and GEM-like structures, named GEMGrid can be integrated over readout chips by means of CMOS post-processing techniques. These devices are intended to improve the performance of Micromegas and GEM detectors placed on top of pixel readout chips. The flexibility of the fabrication process allows to fit the structures on many different pixelized or striped readout chips; aligning the holes of the structure with the pixels of the chip. Furthermore, the grid supporting structures can be sized to fit in between the pixels of the chip, what ensures the complete chip area is available for detection. The final device will consist of a punctured metal film, supported by insulating structures on top of a CMOS chip. Medipix [30], Timepix [31], [32], PSI-46 [33] and GOSSIPO [34] have been used as readout chips.

## 2.2 Fabrication process

This section describes the several post-processing steps applied to the CMOS chips to fabricate amplification grids on top of them. An overview of the process flow is shown in figure 2.14. Prior to any post-processing step the chips are cleaned to improve the adhesion of the posteriorly deposited materials. Fuming nitric acid is used to remove any organic material on the chip surface. The employed microchips (IBM 0.25  $\mu\text{m}$  CMOS) have aluminum bond pads and a silicon nitride anti scratch layer. These layers must remain intact, so the removal of metals in 65%  $\text{HNO}_3$  at 70 °C and hydrofluoric acid cleaning, common in our cleanroom standard cleaning, is not performed.

### 2.2.1 Pad enlargement

Medipix, Timepix and PSI-46 are chips originally meant to be used with a bump bonded silicon sensor on top. For this application pixel pads are made small and have much dielectric surface around. As a result, when employed in gaseous detectors, charge is spread along the amplification path and a part maybe not collected at the pixel pad but adhere to the dielectric surface instead. This will degrade the device sensitivity. Because of this effect, for some chip geometries, increasing the pixel pad area is a requisite. Figure 2.1 shows an optical microscope image of a Timepix chip. Pixel pads and bond pads are clearly distinguished.



**Figure 2.1:** Optical microscope image of a Timepix chip. Pixel pads and bond pads are clearly seen.

After the chip cleaning, it is possible to proceed with the pixel pad enlargement of the readout chip. The pixel pad enlargement is done using a lift-off technique [5]. Two main technology issues would be encountered if a normal metal deposition and etching process was used:

- The difficulty to align the mask for the metal etching if a metal layer is deposited covering all the structures in the finished CMOS wafers.
- The difficulty to etch the metal deposited for the pad enlargement selectively to the underlying metal bond pads of the chip.

For the lift-off process a 13  $\mu\text{m}$  thick layer of AZ-9260 photoresist is spin coated and patterned (figure 2.2). This photoresist is preferred over the more standard Oir 907 photoresist or a specially dedicated lift-off resist as the TI-35. In the first case because metal does not completely lift-off and remains over the wafer if a thin photoresist layer is used; in the second case due to the larger number of processing steps.

Once the resist has been exposed and developed a 500 nm thick layer of aluminum is deposited by sputtering. The metal lift-off step is done in an acetone ultrasonic bath.

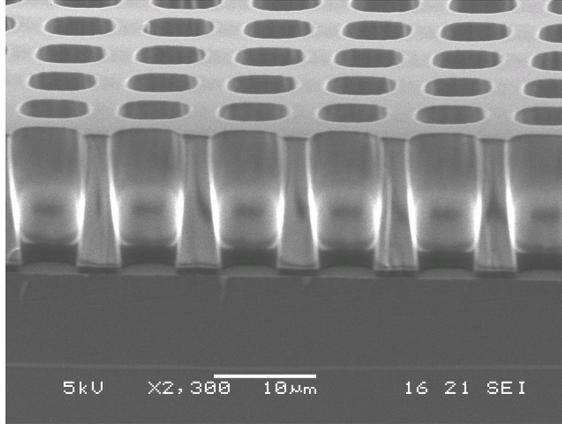
Figure 2.3 shows an optical microscope image of the PSI-46 chip before pixel pad enlargement (left) and after pixel pad enlargement (right).

### 2.2.2 Spark protection

After the pixel enlargement has been done, an anti-spark layer must be deposited on the chip. Silicon rich nitride and hydrogenated amorphous silicon have been used for this purpose. The purpose and properties of this layer will be discussed in chapter 4.

### 2.2.3 Supporting dielectric

For the construction of the insulating support structures SU-8 photoresist [35] was chosen. SU-8 is a negative tone photoresist widely used for high aspect ratio structures in the MEMS community. Its formulation contains the SU-8 polymer (Bisphenol A Novolak epoxy oligomer), a photoacid generator (triarylsulfonium hexafluoroantimonate salt) and the solvent ( $\gamma$ -Butyrolactone) [36]. After exposure to UV light, the photoacid generator decomposes to initiate a crosslinking reaction. This reaction is accelerated with a post-exposure bake. Crosslinking at room temperature is also feasible [37]. Each SU-8 molecule has eight dangling



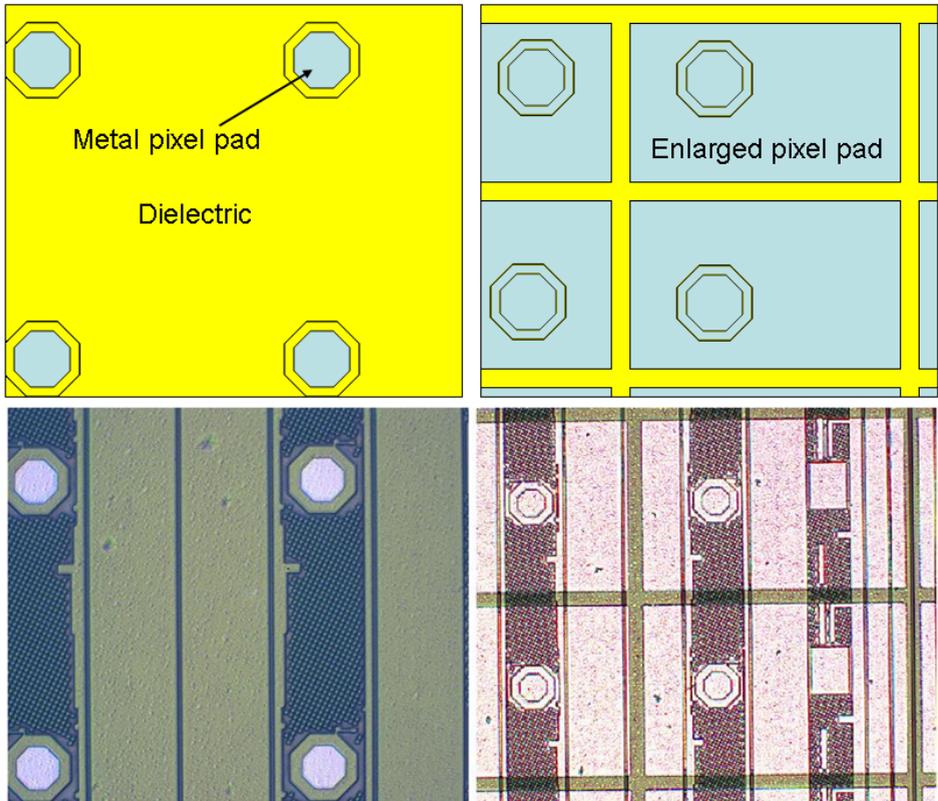
**Figure 2.2:** SEM picture of a  $13\ \mu\text{m}$  thick AZ-9260 photoresist mold employed for the pixel enlargement made by lift-off.

epoxy groups that will interconnect to other molecules after photothermal activation giving a highly cross-linked structure. This property makes SU-8 a very stable resist. Crosslinked parts are not soluble in the SU-8 developer, and if they must be stripped, due to the high level of crosslinking, techniques like RIE plasma ashing, laser ablation or pyrolysis must be employed.

SU-8 can be bought in different premixed formulations. SU-8 50 was used for the fabrication of the support structures. Microchem has currently other SU-8 formulations available, SU-8 2000 and SU-8 3000, formulated with a different solvent. These new formulations are intended to reduce processing time and improve adhesion.

SU-8 presents several characteristics that make it very suitable for our application:

- It can be used both as sacrificial material and structural support [38].
- The layer thickness that can be produced, from  $2\ \mu\text{m}$  to  $3\ \text{mm}$ , is well in the range needed for our detectors [39].
- The thermal budget during its processing, below  $95\ ^\circ\text{C}$  makes it perfectly CMOS compatible [40].



**Figure 2.3:** Top: Schematic figure of a chip before pixel enlargement (left) and after pixel enlargement (right). Bottom: Optical microscope image of the PSI-46 chip before pixel enlargement (left) and after pixel enlargement (right).

- Its use has been previously reported in the construction of gaseous detectors [41].
- It is radiation hard [42].
- Insulating properties and dielectric strength are adequate for the voltages used in the system [43].
- Outgassing can be limited with proper baking [44].

The complete SU-8 processing takes three days and it is detailed below:

- SU-8 spin coating at 3000 rpm to obtain a 50  $\mu\text{m}$  thick layer.
- Soft bake of the resist (10 minutes 50  $^{\circ}\text{C}$ , 10 minutes at 65  $^{\circ}\text{C}$ , 20 minutes at 95  $^{\circ}\text{C}$  and ramp down to room temperature).
- Exposure of the resist (24 seconds at 12  $\text{mW}/\text{cm}^2$ , near UV broad band 350 nm-450 nm).
- Post exposure bake of the resist (5 minutes 50  $^{\circ}\text{C}$ , 5 minutes at 65  $^{\circ}\text{C}$ , 10 minutes at 80  $^{\circ}\text{C}$  and ramp down to room temperature). Resist is allowed to relax overnight to reduce the amount of residual stress [37]. No development at this step.

SU-8 can accumulate high internal stress leading to cracking in the photoresist [45]. To minimize this risk all the SU-8 processing steps include long waiting times and slow ramping up and down of the temperature.

The SU-8 is used as a sacrificial layer. Therefore its development is postponed to a final stage after the deposition and patterning of the metal mesh.

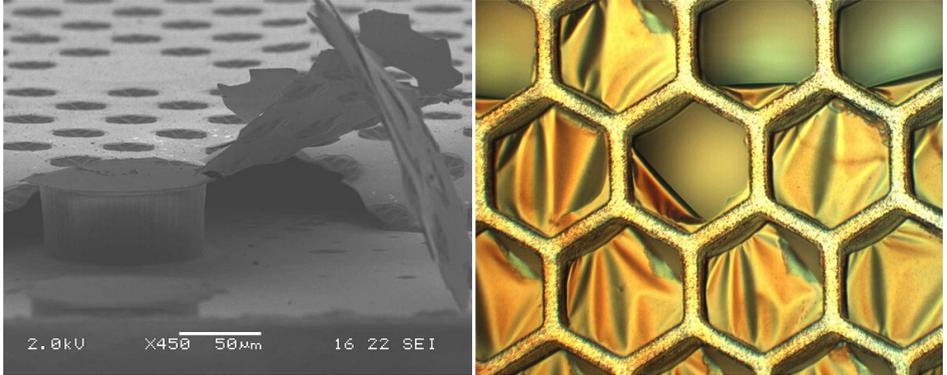
## 2.2.4 Grid electrode

For the conductive metal mesh aluminum is preferred. It can be easily deposited and patterned, it shows low residual stress and adhesion with SU-8 is good [46]. Aluminum was deposited by sputtering in several short steps to reduce the residual stress [47]. The wafer was taken out to the load lock of the sputtering system and vented with nitrogen to cool down the wafer after every deposition.

Deposition of metals over SU-8 can induce crosslinking on the top layer of the resist due to UV light in the plasma and energy released during the deposition. Figure 2.4 shows an early design where the holes in aluminum grid are closed by a thin layer of cross-linked SU-8. To overcome this problem, reports in the literature about the use of thermal evaporation [48], an antireflective coating layer [49] or a buried metal layer [50] can be found. Thermal evaporation of titanium, zinc and aluminum was essayed on top of SU-8; but still a crosslinked SU-8 top layer is formed. The antireflective coatings are usually patterned using dry etching techniques. This would crosslink the SU-8. The printing transfer of a metal layer from a stamp to the SU-8 was not essayed. Although promising, the technique increases the complexity and number of steps of the process.

We have opted instead for the deposition of a 2  $\mu\text{m}$  thick layer of positive photoresist Oir 907-17. This resist is exposed together with the SU-8 and traps part

of the energy involved during the metal deposition; avoiding the total crosslink of the top part of the SU-8.



**Figure 2.4:** SEM picture of a metal grid with closed holes because of a top layer of crosslinked SU-8 (left). Optical microscope image of closed holes because of a layer of crosslinked SU-8. Note some of the holes start to be open (right). Pictures taken by A. A. I. Aarnink.

### 2.2.5 Wafer dicing

The dicing of the devices is one of the open issues in the fabrication process. Due to the relative fragility of the  $1\ \mu\text{m}$  thick metal grid, wafers must be diced into individual chips before the SU-8 development. Devices with a free standing mesh would not survive the high speed water splashing during saw dicing. In our cleanroom only saw dicing was available.

The process to separate the wafer into individual devices depends on the kind of device. Different solutions can be found in the literature. The use of DRIE (Deep Reactive Ion Etching) to etch through the back of the wafer and separate the devices has been shown [51]. Partial wafer dicing, device release at wafer scale and break apart of the chips has also been reported [13]. Laser dicing and partial dicing are options that still should be studied in our case. Stealth dicing [52] is a completely dry process that apparently does not generate debris. This may be an ideal method to dice the chips after grid release at wafer scale.

After the dicing, the individual chips are detached from the dicing foil and stored for the next step: the SU-8 development.

### 2.2.6 SU-8 development

The complete structure is developed in acetone to remove the unexposed SU-8. A final bath in Microstrip 5010 ensures the total opening of the grid holes. Stiction problems [53] during the development were found in the very early designs when the SU-8 pillars were spaced far apart. In the design adapted to the readout chip, the pillar pitch was reduced to  $110\ \mu\text{m}$  -  $165\ \mu\text{m}$  and stiction problems were not encountered.

As the devices are unpackaged, contamination and humidity must be controlled. A gel pack is used for transportation of the chips. They are stored inside a nitrogen filled box.

A schematic of the complete fabrication process is shown in figure 2.14 at the end of the chapter.

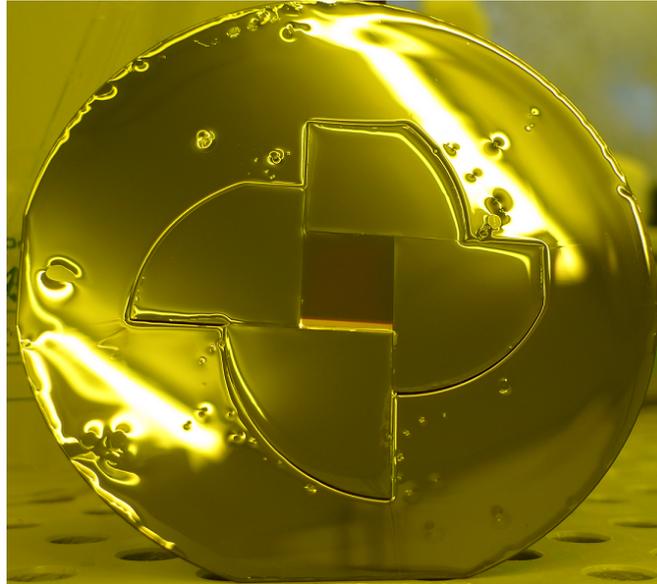
## 2.3 Single chip processing

Large quantities of Medipix2 chips were available during the realization of this project. Complete 4-inch Medipix2 wafer post-processing was possible. On the contrary, limited number of Timepix chips were at our disposal. The post-processing of single Timepix chips was a must to keep the research going. When spin coating photoresist a considerable thickness increase is produced at the circumferential edge of the substrate. This is normally referred as "edge bead". The edge bead makes the rest of the process more critical. Problems arise to expose and bake the photoresist homogeneously. This was not a problem when working with complete wafers as the edge does not contain usable chips. But when working with single chips all the area must be used. Figure 2.6 (left) shows the profile at the edge of the chip after SU-8 spin coating; showing thickness increase at the edge of the chip of about 40% with respect to the center of the chip. Some chips were successfully processed but big gap variation along the chip surface were encountered. These gap variations produce severe gain variation and thus degrade the detector characteristics.

To avoid the edge bead, some options already presented in the literature have been tried. First, a certain amount of SU-8 was scraped over the chip surface [54] and flatted manually by scraping off the excess resist. The edge bead is reduced but it became difficult to control the layer thickness. In figure 2.6 (middle) the SU-8 profile is seen after using this method.

Another option already reported is to dig a trench in a chip holder and glue the chip in place, so that the chip lies flush with the surface of the chip holder [55]. This option was discarded due to the increase in the manufacturing steps,

but a reduced edge bead can be obtained with this technique. The better solution found to reduce the edge bead was to glue the single chip in the center of a carrier wafer. Dummy pieces of  $750\ \mu\text{m}$  height, the same thickness as Medipix and Timepix chips, were glued around the chip to get a flat surface. Figure 2.5 shows a picture of a Timepix chip glued in the center of a carrier wafer. Dummy pieces are glued around the chip. SU-8 has been already spin coated on the structure.

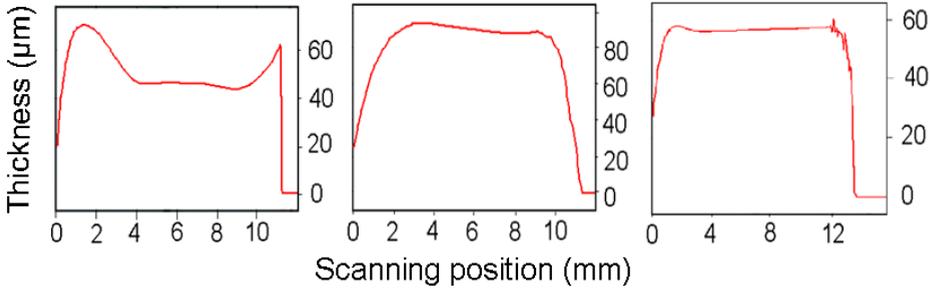


**Figure 2.5:** A Timepix chip glued in the centre of a carrier wafer. Dummy pieces are closely glued around the chip to minimise the edge bead. At this step SU-8 has been already spin coated on the wafer.

After spinning resist on this stack the SU-8 presents a reduced edge bead (figure 2.6 (left)). The rest of the process can be performed comfortably.

SU-8 was also used as glue. When cured at  $120\ ^\circ\text{C}$  for two minutes SU-8 hardens. A strong bond is then formed between chip and carrier wafer.

Before the SU-8 development, the single chip must be released from the carrier wafer. Two methods were developed. Dicing at the edge of the chip through the stack formed by dummy pieces and carrier wafer. In this case, a carrier wafer piece will remain beneath the chip. Heating up the wafer at  $95\ ^\circ\text{C}$  makes the SU-8 soft

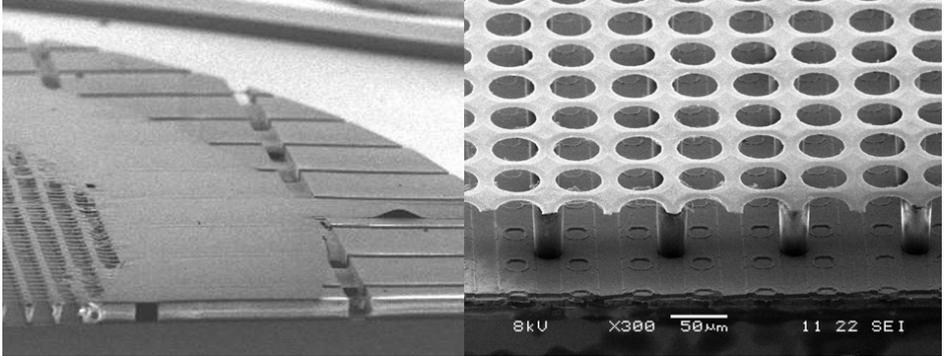


**Figure 2.6:** SU-8 profile measured with a Dektak profilometer at the edge of the chip after spinning resist on a single chip (left), scraping resist over the chip (middle) and with dummy pieces around the chip (right). Edge of the chip is positioned at 0 mm.

again. The chip can be then pushed and released from the carrier wafer. The latter was the most commonly employed solution. Risk of mechanical damage is less than when using saw dicing.

## 2.4 InGrid: an integrated Micromegas-like structure

Following the previously described fabrication process a Micromegas-like structure, named InGrid, can be built. In this kind of structure SU-8 pillars with a pitch of  $110\ \mu\text{m}$  fitting the pixel pitch of the chip, support a metal mesh with holes of  $40\ \mu\text{m}$  diameter. Holes in the grid are perfectly aligned to the pixels of the chip which optimizes detection efficiency. The Moiré effect, produced by the different pitch of Micromegas foils and readout chip [29], is not present. The areas not available for detection, produced by the Micromegas pillars on top of pixels and big supporting frames, are eliminated. Pillars can be fitted in the middle of four pixels. The supporting SU-8 frame at the edge of the detector (see figure 2.7 (left)) can be reduced to a few rows. A SEM picture of the final device integrated over a Timepix chip is shown in figure 2.7 (right).



**Figure 2.7:** Left: SEM picture of the detector edge. A SU-8 frame supports the aluminum grid. Right: SEM picture of the integrated device over a Medipix chip. The pillars are fabricated with  $55\ \mu\text{m}$  thick SU-8 being  $30\ \mu\text{m}$  in diameter. The holes in the aluminum grid are  $40\ \mu\text{m}$  in diameter.

### 2.4.1 Metal grid options

In the process described before, the metal grid is made of a  $1\ \mu\text{m}$  thick aluminum layer. Micromegas foils employ a  $5\ \mu\text{m}$  thick copper grid. Other materials rather than aluminum could offer some advantages to the detector performance:

- Metal electrodes with high resistivity can reduce the spark intensity. Also metals with high melting points that can survive a high number of sparks are of interest [56], [57].
- Aluminum is known not to be an ideal material from the ageing point of view [58].
- A thicker grid to obtain a more robust mesh would be desirable. Copper electroplating is typically employed to deposit thick metal layers.

For the previously mentioned reasons several attempts were done to produce grids made of different materials.

A clear possibility to produce a thicker grid is copper electroplating. Figure 2.9 shows a  $4\ \mu\text{m}$  thick grid made out of copper. In this case the seed layer consisted of  $50\ \text{nm}$  sputtered aluminum to improve adhesion and  $100\ \text{nm}$  sputtered copper.

For the rest of materials sputtering was the only available deposition technique. Table 2.1 summarizes the metals employed and the different results obtained. After optical inspection of the wafers most of these attempts were stopped. Samples showed stressed and cracked metal layers after some few hundred nanometers were deposited on SU-8. We note that when those materials were directly deposited on dummy silicon wafers good layers were obtained. Figure 2.8 shows a picture of four wafers after metal deposition. Copper, chromium, titanium and titanium/tungsten were sputtered. The deposition was done on wafers spin coated with SU-8 and with crosslinked areas. Crosslinked SU-8 areas are seen as circles in the wafer. In all cases bubbles and cracks are observed in the layers.



**Figure 2.8:** Picture of four wafers after metal deposition on top of SU-8. From left to right copper, titanium, chromium, titanium/tungsten were sputtered. Layers with cracks and bubbles are observed. The circles in the wafers correspond to the exposed SU-8 pattern.

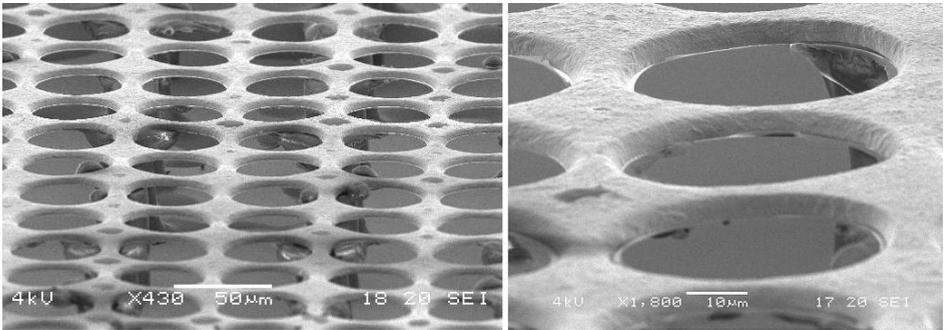
The stress in thin films is well documented by Thornton [59]. In our sputtering system the deposition is made at room temperature. The effect of the thermal stress because of the different expansion coefficient of the SU-8 and the deposited layer is minimal. The layer stress is therefore mainly determined by the intrinsic stress. Generally materials with a higher melting point present higher stress.

Besides the stress another important parameter is the hardness of the SU-8 layer. Not exposed SU-8 is a much softer material than highly crosslinked SU-8. The hardness of SU-8 increases with the crosslinking degree [60]. Optical

Material	Layer thickness	Output
Aluminum	1 $\mu\text{m}$	Good layer
Silver	600 nm	Good layer
Titanium/Tungsten	100 nm	Completely cracked layer
Titanium	130 nm	Wavy layer, bubbles
Sputtered Cu	300 nm	Wavy layer, bubbles
Electroplated Cu	4 $\mu\text{m}$	Good layer
Silicon	300 nm	Cracks in the layer
Gold	300 nm	Wavy layer
Chromium	300 nm	Completely cracked layer

**Table 2.1:** Summary of different metals tried for the grid fabrication and the output results.

inspection after sputtering shows a deformed metal layer in the unexposed SU-8 regions. It is believed the energy of the incoming atoms during sputtering induces deformation in the non crosslinked SU-8 parts. This deformation is transferred to the metal layer (wafer surface can reach more than 60 °C during metal deposition, enough to induce SU-8 reflow). The regions of crosslinked SU-8 did not suffer any stress issue and any metal deposited on top of crosslinked SU-8 performed as well as aluminum.

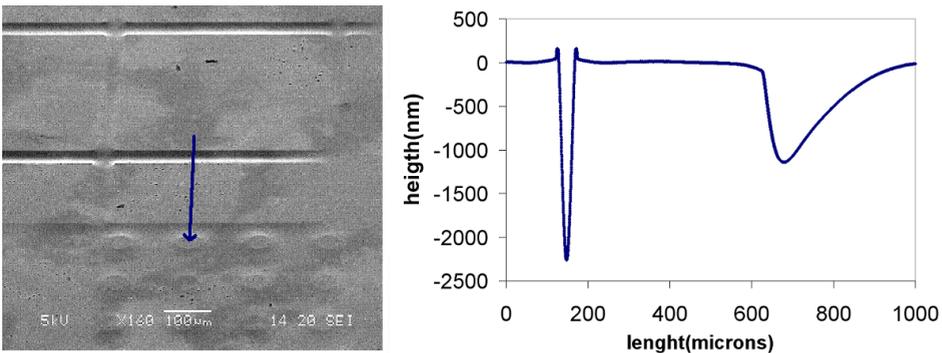


**Figure 2.9:** SEM picture of a 4  $\mu\text{m}$  thick grid made out of electroplated copper using an aluminum/copper seed layer.

We can conclude that grids of aluminum, silver and copper could be produced. Thick copper grids would result in a more mechanically stable detector. From the aging point of view silver seems an attractive material. Devices made out of copper and silver grids have been produced. Radiation tests with these devices have not been performed yet.

### 2.4.2 Surface profile

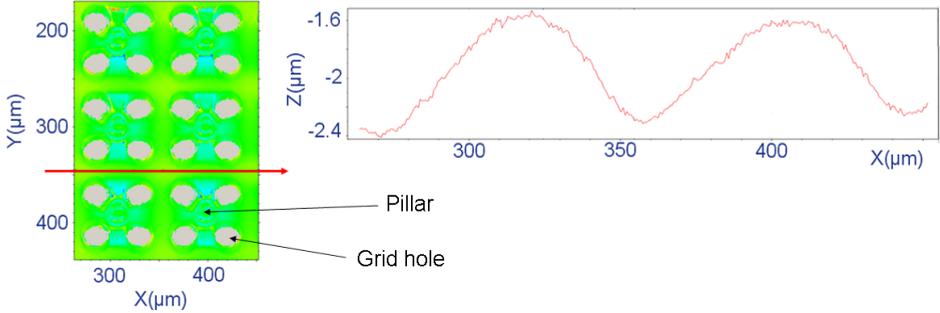
Due to the fact that SU-8 expands after exposure, prior to the metal deposition we already encounter a profile in the SU-8 layer. That profile is produced by the mask exposure pattern. The deposited metal will follow that profile. After the SU-8 development and release of the metal mesh that profile is reflected in the flatness of the grid. Figure 2.10 left shows a SEM picture of a SU-8 structure with exposed and unexposed parts where the different topography is observed (see the profile around the pillars that later will support the grid). In figure 2.10 right that profile was measured with a profilometer showing that the difference in height is between  $1\ \mu\text{m}$  and  $2\ \mu\text{m}$ .



**Figure 2.10:** SU-8 profile after exposure of certain parts. Left: angled view SEM image of the area. Circular pillars and big square dike areas are observed. Right: profilometer measurement along the arrow line in left figure.

After the development of the SU-8 the profile of the metal grid was measured again in a design with  $90\ \mu\text{m}$  pillar pitch,  $45\ \mu\text{m}$  hole pitch and  $15\ \mu\text{m}$  hole diameter. Figure 2.11 shows the metal mesh profile measured with a white light interferometer from Polytec [61]. The roughness, in the order of  $1\ \mu\text{m}$  is in agree-

ment with the profile produced in the SU-8 after exposure. This grid profile should not represent any reduction in the detector performance. Gain in Micromegas-like structures is insensitive to small gap variations [19]. Detectors fabricated with different gap sizes and geometries have shown excellent performance [62].



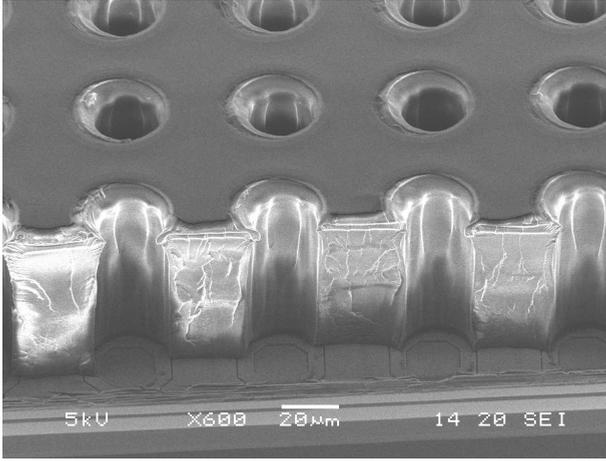
**Figure 2.11:** Mesh roughness across a small area of the device measured with a white light interferometer. The red arrow indicates the scanning position.

## 2.5 GEMGrid: an integrated GEM-like detector

GEMGrid is a GEM-like structure built with the same technology as InGrid. In this GEM-like structure the detector is placed directly on top of the readout chip with no extraction gap between detector and readout chip. The pixels of the chip will act as bottom electrode. Two versions of GEMGrid structures were developed, one having both holes in the SU-8 and holes in the metal the same  $30\ \mu\text{m}$  diameter. The second version has recessed SU-8 where the holes in the metal grid were  $30\ \mu\text{m}$  diameter and the holes in the SU-8 were  $46\ \mu\text{m}$  diameter. This second version is similar to a Micro-bulk Micromegas [63] where instead of pillars supporting the metal mesh those are replaced by a continuous SU-8 wall on top of which the metal grid is placed.

The detector has a structural strength benefit in comparison to InGrid. The device can be handled with a vacuum holder without damaging the metal mesh, something not possible with InGrid structures, and impact problems are improved. This point will be further discussed in chapter 7. Compared with traditional GEM detectors the GEMGrid device allows to perfectly align the holes of the structure with the pixels of the chip. Cylindrical holes can be produced to reduce charging

[64] of the hole side and the diameters of the metal layer hole and the insulator hole can be chosen separately with a high degree of freedom. It is also believed that the photon feed back will be reduced by the structure shape as they cannot travel far without encountering a SU-8 block.



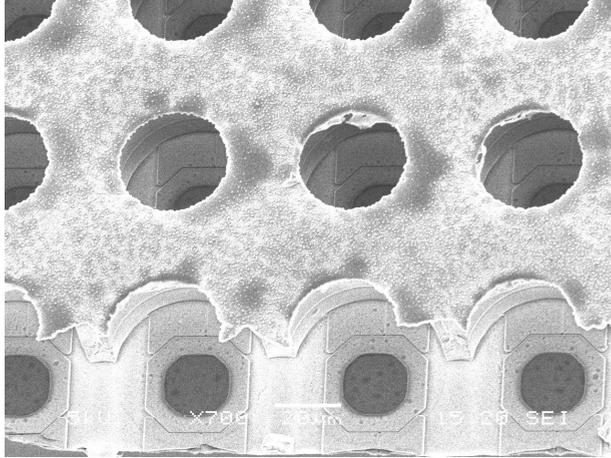
**Figure 2.12:** SEM image of the detector fabricated with  $55\ \mu\text{m}$  thick SU-8 over a Timepix chip. The holes in metal (aluminum) and insulator (SU-8) are  $30\ \mu\text{m}$  in diameter.

The GEMGrid structure has large areas of crosslinked SU-8. The deposition of thick aluminum layers or other metals is feasible on top of crosslinked SU-8. In the InGrid case big areas of unexposed SU-8 are in between sparse pillars. The long sputtering deforms the unexposed SU-8 resulting in an unusable metal layer.

This side benefit of the GEMGrid makes it a solid candidate to investigate the use of other metals or high resistive materials (see chapter 4) as grid layer.

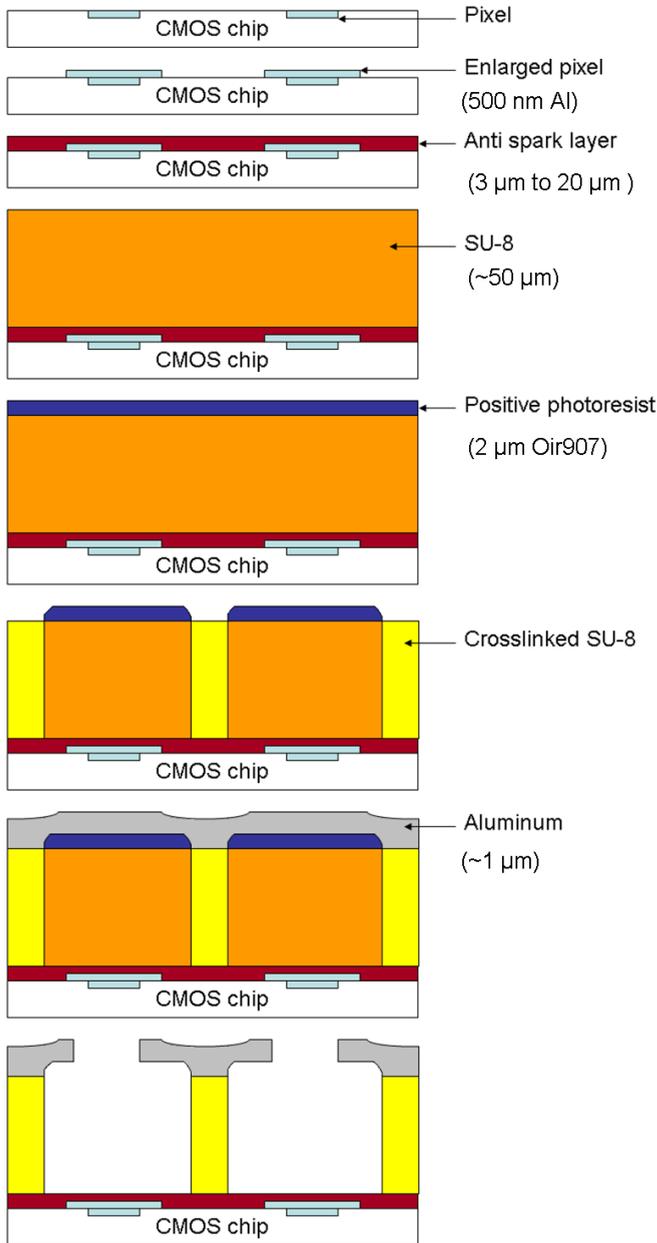
## 2.6 Towards mass production

In following chapters we will present measurement results with InGrid and GEMGrid detectors built by means of wafer post-processing technology. These devices show an excellent performance, but to ensure the success of a detector, a key issue is the possibility to mass produce the detectors in a semi-industrial process. Among other factors, GEM and Micromegas have outperformed many



**Figure 2.13:** SEM image of the modified version of the detector chip with recessed insulator walls over a Timepix chip. The insulator hole diameter is  $46 \mu\text{m}$ , while the metal holes are  $30 \mu\text{m}$  in diameter.

other promising Micro Patterned Gaseous Detectors like micro-gap [65], micro-dot [66], CAT [67], small gap [68], micro-CAT [69], micro-groove [70] and WELL [71], because their feasibility to be produced in enough quantities to supply the demand of several institutes and companies. A collaboration effort is currently ongoing between MESA+ University of Twente, Nikhef, SMC (Scottish Microelectronics Center, Edinburgh) and IZM Fraunhofer Institute in Berlin to post-process full size 200 mm Timepix wafers. This will ensure enough quantities of post-processed chips for large area experiments.



**Figure 2.14:** Schematic of the fabrication process flow. From top to bottom: 1) Naked chip, 2) Pixel enlargement (depending on chip geometry), 3) Anti spark layer deposition, 4) SU-8 deposition, 5) Positive resist deposition, 6) UV exposure, 7) Metal deposition 8) Metal patterning and structure development. The figure is not drawn to scale.

# Chapter 3

## Geometrical design of Ingrid detectors

The work carried out in this chapter presents a study of the influence of the geometry parameters (amplification gap size, hole pitch and hole diameter) of the integrated InGrid detectors on its gain and energy resolution. The different radiation sources employed for the testing of the devices are also explained in this chapter.

### 3.1 Radiation tests

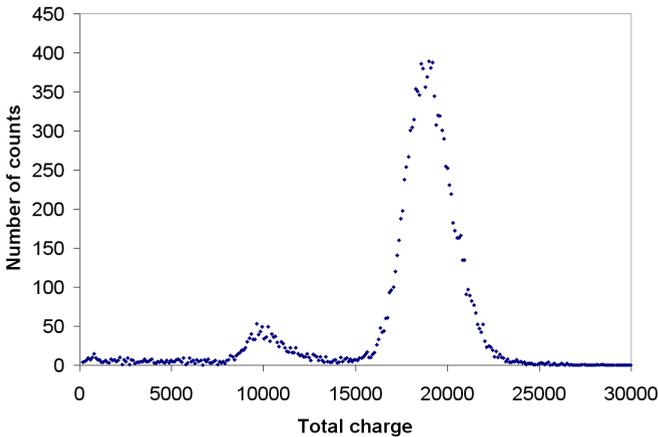
This section is devoted to explain the several radiation tests with energetic particles used to determine the performance of the detectors. In this chapter itself some of the radiation sources are used to determine the response of InGrids on dummy silicon substrates. Other radiation sources are employed in the following chapters.

#### 3.1.1 Irradiation with $^{55}\text{Fe}$

$^{55}\text{Fe}$  is a commonly employed radioactive source. The  $^{55}\text{Fe}$  isotope decays with the emission of photons of 5.90 keV and 6.49 keV in the ratio 8.5 to 1. The  $^{55}\text{Fe}$  source is used as a calibration for the detector. The detector is irradiated with the  $^{55}\text{Fe}$  source through a collimator. Once the photons emitted by the  $^{55}\text{Fe}$

reach the sensitive gas volume they create a cloud of electrons. The mean number of electrons in the cloud depends on the gas mixture. The generated electrons drift toward the amplification region of the detector. In the amplification region the electrons are multiplied exponentially. The movement of ions and electrons induces a pulse at the detector electrodes. The pulse height depends on the amount of electrons created in the  $^{55}\text{Fe}$  photon conversion in the gas and the gain of the detector. A pulse height spectrum is typically made to assess the performance of the detector.

In argon based mixtures  $^{55}\text{Fe}$  produces a very recognizable spectrum. That spectrum has been shown by all type of gaseous detectors. Figure 3.1 shows a typical  $^{55}\text{Fe}$  spectrum recorded with an InGrid detector. From the width of the main peak the energy resolution of the detector is deduced. An energy resolution in the order of 12% FWHM indicates a good detector. The source is also used to measure the gain of the detector. Extensive  $^{55}\text{Fe}$  spectra are shown in following chapters. More details can be found in reference [62].



**Figure 3.1:** Typical  $^{55}\text{Fe}$  spectrum recorded with an InGrid detector in  $\text{Ar}/i\text{C}_4\text{H}_{10}$ .

### 3.1.2 Irradiation with $^{90}\text{Sr}$

$^{90}\text{Sr}$  is a strontium isotope that decays through beta decay. In the process an anti-neutrino and an electron are emitted. Emitted electrons have a continuous

energy spectrum with a mean value of 2.2 MeV. Electrons emitted from  $^{90}\text{Sr}$  traverse the gas over the detector and create a track of electrons. That track can be imaged with InGrid detectors. Some examples of tracks produced by electrons emitted by  $^{90}\text{Sr}$  are shown in chapter 5. The  $^{90}\text{Sr}$  radioactive source is used to evaluate the track reconstruction capabilities of the detector. As electrons are separated along the track it is used to determine for a given voltage the efficiency of the device to detect single electrons.

### 3.1.3 Alpha particles

Alpha particles are nuclei of helium emitted by means of alpha decay from radioactive nuclei. They have a high ionizing power and low penetration depth. Typically they can be stopped by a sheet of paper. Alpha particles produce an important density of charge during ionization. That means that after amplification in the detector a great amount of charge will be produced. Therefore alpha particles produce a large pulse signal. Alpha particles are prone to trigger discharges. More details will be given in chapter 4.

### 3.1.4 Cosmic rays

Cosmic rays are energetic particles coming from outer space. When cosmic rays interact with the atmosphere they create a shower of particles. Those particles arrive to the surface of the Earth and interact with matter. For our experiments a setup was specially mounted to detect secondary cosmic rays (mainly muons). Two scintillators are placed over and under the detector. They give a trigger signal when a cosmic ray traverses them. The trigger indicates a cosmic ray has passed by the detector area. At that moment the detector can be readout and the image of the particle recorded. Cosmic rays are employed as a natural source to determine if the device can detect minimum ionizing particles. In chapter 5 examples of cosmic ray tracks are shown.

## 3.2 InGrid gain and energy resolution

Gain, gain homogeneity and energy resolution of InGrid detectors with different geometry parameters were studied. For this purpose several InGrid detectors were fabricated on dummy silicon wafers with a metalized anode. This is a necessary study to determine which geometry will produce the best performance when the device is integrated on a CMOS chip. The results were presented at the 8th International Workshop on Radiation Imaging Detectors (IWORID) and published

in Nuclear Instruments and Methods in Physics Research Section A: accelerators, spectrometers, detectors and associated equipment. This publication is reprinted in this chapter with permission of Elsevier Publishers.

A more thorough analysis of the findings was later made by M. Chefdeville and presented in his Ph.D. thesis (January 2009) [62].

# On the geometrical design of integrated Micromegas detectors

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## Abstract

This paper presents the operational characteristics of several integrated Micromegas detectors. These detectors called InGrids are made by means of micro-electronic fabrication techniques. These techniques allow a large variety of detector geometry to be made and studied. Gain, gain homogeneity and energy resolution were measured for various amplification gap sizes, hole pitches and hole diameters in Argon/Isobutane. Gain measurements as a function of gap thickness are compared to the Rose and Korff formula and a model of the detector gain. Our model uses electric field maps and MAGBOLTZ calculated amplification coefficients.

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Keywords: Integrated Micromegas; Wafer post-processing; Gain; Energy resolution

## 1. Introduction

Microfabrication techniques have dramatically improved the performance of gaseous detectors. Devices such as Micromegas [1] and GEM [2] make use of these techniques during their fabrication process to achieve high granularity, homogeneity and good spatial resolution. Punctured membranes can be produced with high precision, and hole sizes and pitches can be adapted easily to the specific needs. But despite using high accurate techniques to build the detector itself, the final mounting step over the readout plane is made manually. This inherently comes with several disadvantages, like misalignment between holes and pixels, Moiré effect, dead pixel areas, human errors and problems to reach volume production.

The successful realization of the InGrid detector by Chefdeville et al. [3] is a major step towards the fully integrated gaseous detector. The process is IC compatible so the grid can be integrated directly on a pixel readout

chip in a wafer post processing step with good alignment between holes and pixels. The pillar diameter can be shrunk to 30  $\mu\text{m}$  so that the pillars fit in between the grid holes resulting in 100% detection area. Both the pillar height (amplification gap) and the grid design (hole shape, pattern and size) can be accurately controlled. This offers new design space for the detector optimization.

In this work, several InGrid prototypes have been made and their operational characteristics measured. The experimental setup and fabrication process were presented in Ref. [3]. All measurements have been done using an 80/20 Argon/Isobutane gas mixture. The next section describes our approach to model the detector gain. Sections 3–6 discuss gain and energy resolution measurements and modelling results.

## 2. Gain modelling

Under the assumption that secondary processes and attachment are negligible, the gas gain in a high electric field is governed by the primary Townsend coefficient  $\alpha(E)$ , the mean number of ion pairs formed per unit length by an electron at an electric field  $E$ . A single electron traversing a path along the  $z$  direction will on an

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average cause a total gain  $G$  of

$$G = e^{\int \alpha(E(z)) dz}. \quad (1)$$

In the case of a homogeneous electric field,  $\alpha$  is constant and the equation simplifies to

$$G = e^{\alpha g} \quad (2)$$

with  $g$  the projected track length (the distance between the two plates in a parallel-plate geometry).

The electric field in the Micromegas detector is generally approximated as a composition of a homogeneous low-(drift) field region ( $E_d$ ) and a homogeneous high-field region ( $E_a$ ). This assumption allows to define the field ratio ( $E_a/E_d$ ) and to model the collection efficiency and the ion backflow in terms of this field ratio. In this study, we found the precise field shape at intermediate-field strength (i.e. near the foil openings) to be crucial for the overall detector performance, see Sections 3 and 5.

To estimate the gain of a Micromegas detector, the Townsend coefficient then must be integrated along the electron drift path. The statistical variation in electron trajectories and collision phenomena is accounted for by Monte Carlo calculations as provided by the program GARFIELD [4], using the electric field maps from MAXWELL 3D [5] and amplification and drift coefficients from MAGBOLTZ [6].

### 3. Gain homogeneity

The microelectronic fabrication techniques (spin coating, sputtering and wet etching) used to make the InGrids allow an accurate control of the gap thickness, the grid thickness and the hole diameter, resulting in a very good gain homogeneity (defined as the RMS relative variation of gas gain across a prototype).

For several InGrids, the gain was measured on 10 equally spaced locations across the active area by means of a collimator. The homogeneity was found to be 10% in the worst case and 1.6% in the best one (Fig. 1).

For a given gap thickness, the gain homogeneity was measured to degrade for larger hole diameters. Inversely, for a given grid geometry, it was improving for smaller gap thicknesses. We believe the gain to be more sensitive to

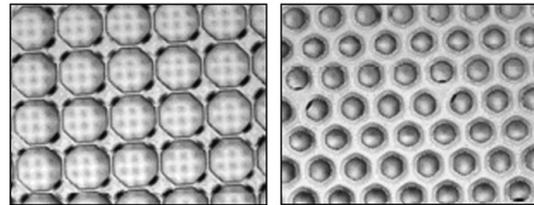


Fig. 1. An 80- $\mu\text{m}$  hole pitch, 75- $\mu\text{m}$  gap InGrid, showing 10% gain homogeneity (left side) and a 60- $\mu\text{m}$  hole pitch, 35- $\mu\text{m}$  gap InGrid exhibiting 1.6% gain homogeneity with a 240- $\mu\text{m}$  pillar pitch (right side).

Table 1  
Gain sensitivity to hole diameter variations

Hole $\varnothing$ ( $\mu\text{m}$ )	$\Delta\varnothing/\varnothing$ (%)	$\Delta G/G$ (%)
36	10	19
	-10	6
70	10	30
	-10	19

Table 2  
Gain sensitivity to gap thickness variations

Hole $\varnothing$ ( $\mu\text{m}$ )	$\Delta g/g$ (%)	$\Delta G/G$ (%)
36	10	45
	-10	40
70	10	43
	-10	38

hole diameter and gap thickness variations in the case of bigger holes.

This sensitivity difference was simulated using the method described in Section 2. Gains of a large and a small hole configuration of 75- $\mu\text{m}$  gap were calculated. Same operation was done for hole diameters and gap thicknesses differing  $\pm 10\%$  of their original values. Results are summarized in Tables 1 and 2 and show that the large hole configuration is more sensitive to diameter variations while both are almost as sensitive to gap variations.

### 4. Gain and gap thickness

One particularly interesting feature of the Micromegas detector that can be studied with InGrid is the dependence of the gain with the gap thickness. For a given grid voltage, increasing the gap thickness reduces the field but increases the available amplification length [8]. If Eq. (1) holds the gap thickness dependence of the gain will be governed by the field dependence of the Townsend coefficient.

An empirical formula valid for low fields was derived by Rose and Korff [7,8]:

$$\alpha = APe^{-BP/E} \quad (3)$$

where  $P$  is the pressure,  $E$  the electric field strength and  $A$  and  $B$  constants of the gas mixture. Replacing  $E$  by  $V/g$  ( $V$  being the grid voltage) and using Eq. (1) leads to

$$G = e^{gAPe^{-gBP/V}}. \quad (4)$$

For a given gas, pressure and grid voltage  $V$ , the gain presents a maximum for a certain gap thickness

$$g(G_{\text{max}}) = V/(BP). \quad (5)$$

Selecting the gap thickness according to Eq. (5) should make the gain to a certain extent insensitive to mechanical imperfections of the mesh (wrinkles) and of the gap thickness (pillar height variation). This is not a critical

point for the InGrid as gap thickness and grid flatness are accurately controlled. It is however interesting to check that there is indeed a gap thickness for which the gain is maximum.

Several devices with gap thicknesses in the range from 35 to 75  $\mu\text{m}$  have been built and gain curves have been measured. In Fig. 2 gain curves as a function of the grid voltage are shown. The gain curves have been fitted using the Rose and Korff formula.

In Fig. 3 the dependence of gain with gap thickness is presented. These measurements were performed at almost constant atmospheric pressure (variation less than 2%).

From Fig. 3, it is clear that the Rose and Korff formula describes the trend well, even though the fit is not perfect and one requires more measurement points for a critical assessment. The gas gain reaches its maximum value for a gap around 50  $\mu\text{m}$  operated with 450 V on the grid.

### 5. Gain and grid geometry

Gain as a function of grid geometry has been measured for three 75  $\mu\text{m}$  gap InGrids, each having a different hole diameter and hole pitch summarized in Table 3.

The gain is clearly dependent on the hole diameter (Fig. 4). This is understood by looking at the field strength

Table 3  
Measured gain for different InGrid geometries

	InGrid 1	InGrid 2	InGrid 3
Hole pitch ( $\mu\text{m}$ )	50	60	80
Hole diameter ( $\mu\text{m}$ )	32	36	75
Gain at 500 V	9800	9900	2900

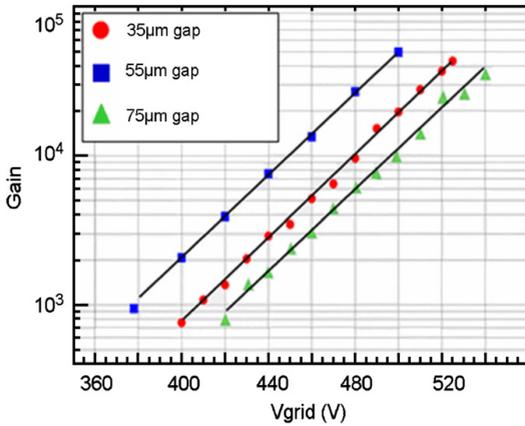


Fig. 2. Gain as a function of grid voltage for various gap thicknesses. The data points are fitted using the Rose and Korff formula (lines).

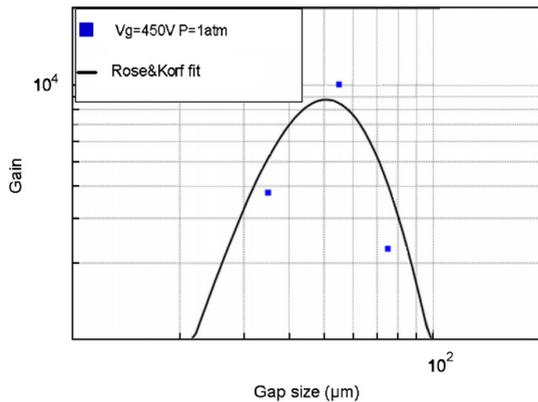


Fig. 3. Gain at 450 V on the grid for various gap thicknesses. The data points are fitted using the Rose and Korff formula.

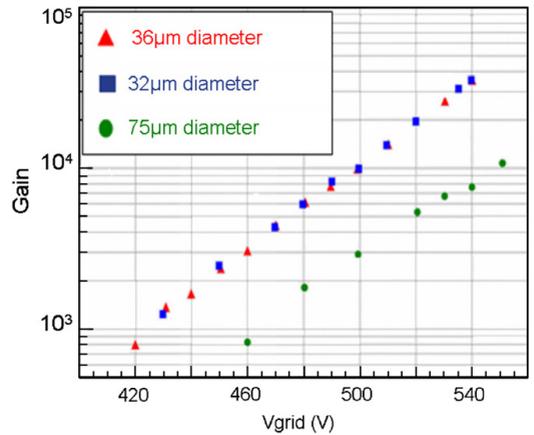


Fig. 4. Gain for three grid geometries (see Table 3).

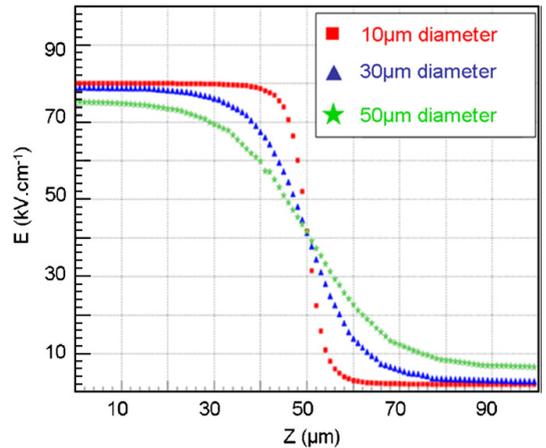


Fig. 5. Electric field along the hole axis of a 50- $\mu\text{m}$  gap InGrid for various hole diameters (400 V on the grid).

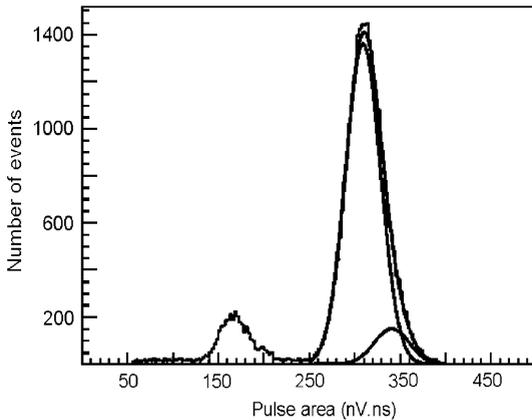


Fig. 6.  $^{55}\text{Fe}$  spectra in Argon showing the fit of the 5.9 and 6.5 keV lines.

along the hole axis for different hole diameter, keeping the hole pitch fixed (Fig. 5). While decreasing the hole diameter, the electric field along the hole axis is higher over a longer distance, therefore the overall gain increases.

## 6. Energy resolution measurements

The resolution of gaseous detectors is mainly determined by the primary charge fluctuations and the single electron gain fluctuations. These sources are intrinsic to the sensing gas and cannot be avoided. On the other hand, fluctuation sources like attachment and collection efficiency depend on the drift field and can therefore be optimized for minimum energy resolution.

Energy resolution is calculated using  $^{55}\text{Fe}$  spectra.  $^{55}\text{Fe}$  emits quanta of 5.9 and 6.5 keV in the ratio 9–1. This ratio is slightly modified to 7.5–1, due to the different absorption of these lines in the gas [7]. Spectra were fitted using two Gaussian functions (Fig. 6). The parameters (mean, height, width) of the 6.5 keV line were fixed by the ones of the 5.9 keV line. The energy resolution is defined as the FWHM of the 5.9 keV line.

For the three grid geometries tabulated in Table 3, the energy resolution was measured as a function of the grid voltage. Remarkably, the three curves almost superimpose when plotted as a function of the gain (Fig. 7).

As already noted in Ref. [9], the resolution exhibits a minimum with respect to grid voltage (or gain). An explanation of the resolution improvement could be the reduction of avalanche fluctuations when increasing the amplification field i.e. transition from exponential to Polya single electron gain fluctuations. Degradation above a gain of  $5 \times 10^3$  could be explained by secondary avalanches induced by UV photons or space charge effects that distort the field.

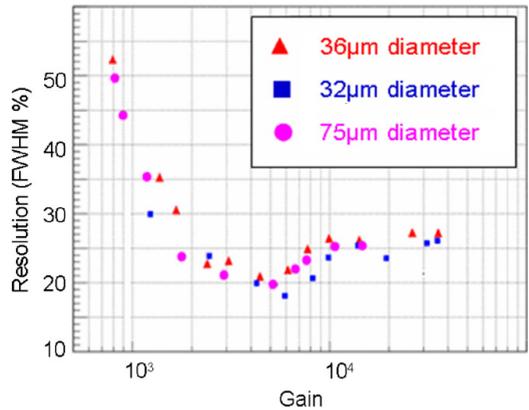


Fig. 7. Resolution vs. gain for various hole diameters.

## 7. Conclusions

The fabrication process of InGrid has reached a mature level and several InGrids of different geometry have been made and tested. Excellent homogeneity of the gas gain across a detector (1.6% RMS) is reported. Gain measurements for different amplification gap thicknesses show a good agreement with the Rose and Korff formula. Energy resolution has been measured to have a minimum at a gain around  $5 \times 10^3$  for three 75- $\mu\text{m}$  gap thickness InGrids of different hole pitch and diameter. The obtained results further show that considerable design freedom exists in the hole shape and diameter.

## Acknowledgements

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# Chapter 4

## Spark protection of MPGD's

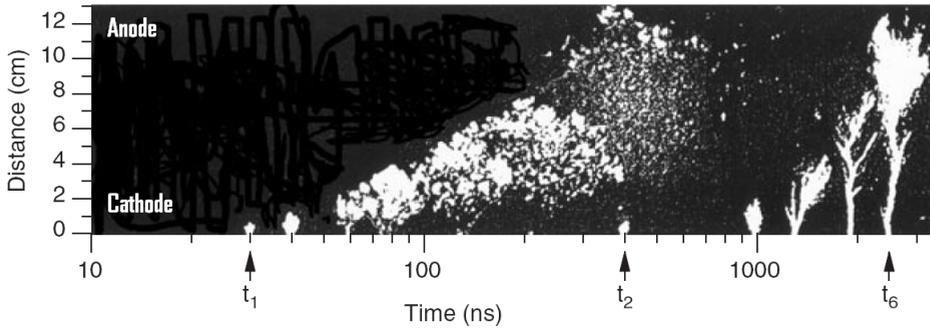
In this chapter spark damage in gaseous detectors is discussed. A method to protect the readout electronics is presented. Two materials, hydrogenated amorphous silicon (a-Si:H) and silicon rich nitride (SiRN) have been deposited on top of Medipix and Timepix chips. Those chips have survived the previously lethal discharges.

### 4.1 Introduction

A common problem associated with gas-filled proportional chambers is sparking. We understand a spark or discharge as the development of a conductive and self-sustained plasma between two electrodes. Sparks are initiated by a streamer formation. A description of the streamer behaviour can be found in reference [72]. A streamer is a pre-plasma filament connecting anode and cathode of the detector.

Streamers are triggered in the presence of high electric fields when the space-charge distribution in the head and tail of the avalanche increases locally the electric field. In these conditions, photoelectrons are created outside the avalanche from the photoionization of the gas or the cathode or by ion bombardement of the cathode. Those electrons move towards the avalanche and contribute to its development and to maintain the streamer expansion at the back front. The avalanche grows in all directions and a pre-plasma filament is formed. When the streamer connects anode and cathode a spark may happen. Figure 4.1 shows a

picture of the evolution from a streamer into a spark from cathode to anode [73]. Streamers from anode to cathode and in both directions have also been recorded [74].



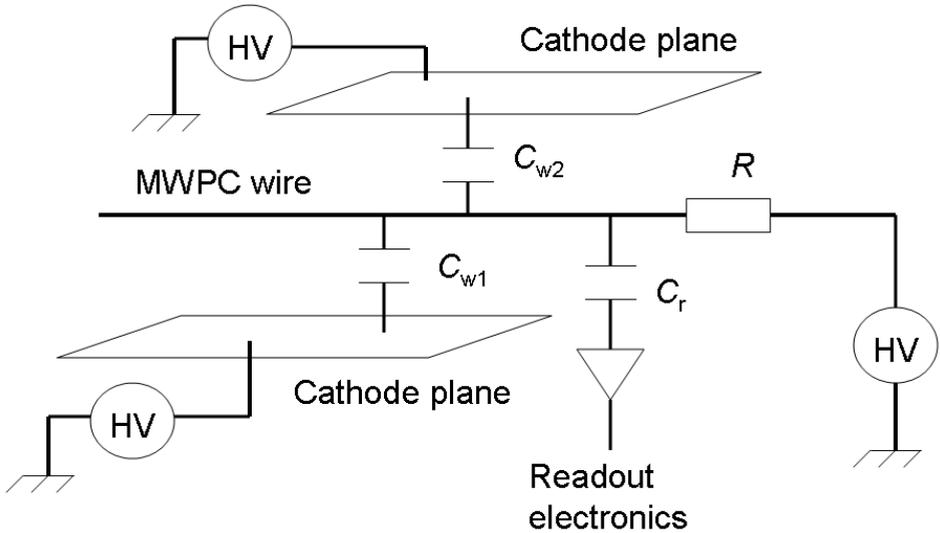
**Figure 4.1:** Typical sequence of shutter photographs of the cathode-directed streamer in pure  $N_2$  gas (From Dale, fig 5.39 in [73].)

The physical origin of the discharges may depend on several causes [75]:

- Breakdown produced by photon feedback.
- Corona discharges due to sharp edges in the detector.
- Discharges because of avalanche gain fluctuations.
- High-rate induced breakdown.
- Breakdown induced by highly ionizing particles.

All the previous mechanisms point to the same generally accepted physical picture. When the total charge density in an avalanche becomes higher than  $10^7$ - $10^8$  electron-ion pairs (known as the Raether limit [76], [77]) the electron avalanche may evolve into a discharge. The density and energy of the participating electrons becomes high, forming a conductive plasma. This creates a conducting path between the participating electrodes.

Figure 4.2 shows a schematic of the electrical connections of a wire in a Multi wire proportional chamber (MWPC). High voltage is supplied to the wire through a resistor. A capacitance is formed between the wire and the anode planes. A capacitor is connected to the wire to readout the signals.

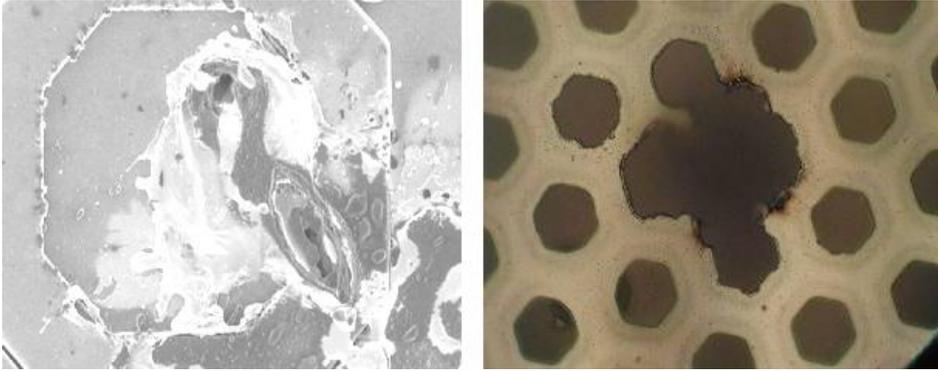


**Figure 4.2:** Schematic view of the electrical connections in a wire of a MWPC. The high voltage is supplied through a resistor. A capacitance is formed between the wire and the cathode planes. Signals are readout through a capacitor connected to the anode.

Normally the discharge is finished when the spark current leads to a reduction in the electric field. Any current drawn from the electrode leads to a voltage drop over the resistor. The voltage reduction at the wire leads to a decrease in the electric field. The drop in the electric field leads to a local gain reduction. The electron-ion pair density is decreased and the Raether limit is crossed down. This self-quenching is observed in most gaseous detectors where the electrodes are connected to the high voltage supply via a  $\sim 1 \text{ M}\Omega$  resistor. More details can be found in [77].

Due to the discharges electrodes in the detector may get damaged (partially molten). Deposits can also occur. This is more acute in MPGDs than in classical wire chambers. MPGDs have electrodes with smaller volume than wire chambers to dissipate the heat produced by a discharge. Figure 4.3 left shows a pixel of a Medipix chip perforated by a spark. In our early experiments unprotected chips could not be operated longer than a couple of hours. Figure 4.3 right shows a damaged grid after a discharge; a part of the aluminum mesh has been molten.

Even if the electrodes are protected with a high melting point material another possible damage produced by sparks is an excess of charge dumped in the detector that can destroy the readout electronics.



**Figure 4.3:** SEM image of Medipix2 chip perforated by a spark (left). Optical microscope image of an aluminum grid molten by a discharge (right).

To overcome the spark problem several groups have worked on different solutions to reduce the spark probability:

- Multilayer structures where the gain per stage is reduced and charge is spread. A multiple GEM stack is the most popular [25].
- A gas mixture with very good quenching properties that can reduce the spark probability [78].

Several known solutions exist to limit its damage once a spark appears:

- Metal electrodes with high resistivity that reduce the sparks intensity. Also metals with high melting point that can survive a high number of sparks are used [56], [57].
- A current limiting circuitry [79].
- A heat dissipating pn junction connected to the pixel input pad of pixel readout chips. This heat dissipating circuitry will be used in the Medipix3 chip.

- A segmentation of the readout anode in strips. The voltage is provided to every strip through a resistor and readout through a capacitor. This way the complete mesh is not discharged in a single spark, what limits the capacitively stored energy per discharge [77]. The capacitance  $C_{w1} + C_{w2}$  in figure 4.2 is reduced.

Sparks can always be triggered by heavily ionizing particles so it is difficult to completely suppress them. It would be preferable to build a spark proof detector.

In Resistive Plate Chambers [80], with one or both electrodes made of a high resistive material this is the case. The instant drain of the charge deposited by the discharge is intrinsically blocked. The not drained-off charge creates a compensating electric field that produces a local drop in the applied field. This causes a self-quench of the discharge. Its amplitude, typical a fraction of the charge stored in the assembly of the participating electrodes, is reduced [81].

In a first approximation the resistive layer can be modeled as a capacitor and a resistor in parallel. In this simplified model any resistive layer has a characteristic RC time. It can be associated with the recovery time of a potential change of the layer surface. A complete detailed study can be found in [82] [83].

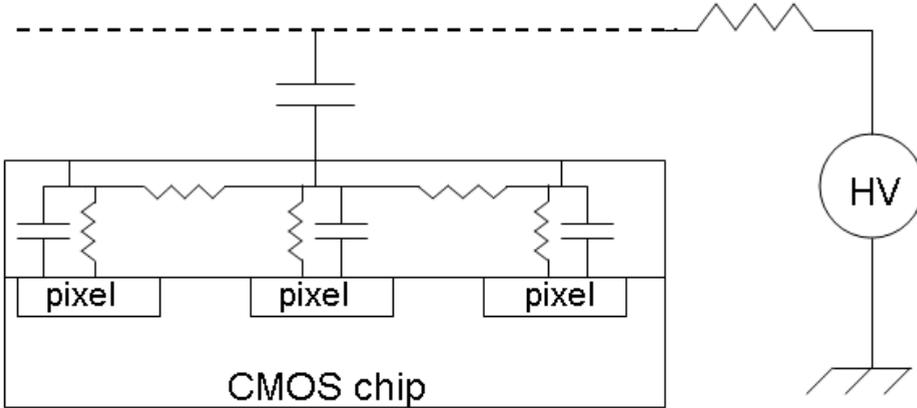
Our high resistive layers could not be patterned, therefore the layer connects all the pixels and a lumped circuit must be used to describe the layer. Figure 4.4 shows an equivalent circuit of the detector. In our detectors, a variation of 18 volts in the potential difference between the grid and layer surface results in a factor two in gain [62]. The specific resistivity of the layer material should be low enough in order to limit the potential drop of the layer surface, due to the vertical current across the layer, to  $\sim 1$  volt, therefore not affecting the gain. The average current flowing from the chip into the gas equals the pixel hit rate times the gain times the charge of the electron. For sLHC<sup>1</sup> applications the specific resistivity of the layer material should be as low as  $10^9 \Omega \cdot \text{cm}$ . For less high-rate applications, layer materials with a specific resistivity in the range of  $10^9 - 10^{13} \Omega \cdot \text{cm}$  can be applied, and the value is not critical.

The resistance between adjacent pixel input pads should be sufficiently high: to limit the conductivity between adjacent pixels. This value should be higher than  $100 \text{ M}\Omega$ . This sets a limit to the minimum specific resistivity of the applied material of about  $10^5 \Omega \cdot \text{cm}$ . The quenching power of a protection layer is determined by the local reduction of the electric field due to the charge deposited during a discharge. The field reduction in the avalanche gap equals  $Q_a \cdot D / (\epsilon_0 \cdot k \cdot G)$ , where  $Q_a$  equals the charge deposited onto the layer surface,  $D$  equals the layer

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<sup>1</sup>A plan to upgrade the Large Hadron Collider to higher luminosity, see reference [84].

thickness,  $k$  the relative permeability of the layer material, and  $G$  the thickness of the avalanche gap.



**Figure 4.4:** Equivalent circuit of the detector. The high resistive layer is modeled as a capacitor and resistor in parallel. A capacitance is formed between the grid and the anode.

It is attractive to pursue the combination of the protection given by RPCs with the high counting rate provided by MPGDs. This has been previously reported using a mixture of epoxy and ink that produces a rubber like material. Its resistivity can be varied from  $10^7 \Omega \cdot \text{cm}$  to  $10^{12} \Omega \cdot \text{cm}$  to cover the metallic electrode of a parallel mesh chamber [85]. High counting rates and spark protection are obtained.

Also the use of high resistivity diamond-like-carbon (DLC) has been reported. MSGCs over-coated with DLC having resistivities varying from  $10^{14} \Omega/\text{square}$  to  $10^{16} \Omega/\text{square}$  seem to be protected against discharges [86].

Recently the same concept has been applied to MPGDs. GEMs with high resistive electrodes have been developed. First tests show that sparks in these detectors do not damage the electrodes or the readout electronics [87].

The success obtained with other technologies encouraged us to employ a similar high resistive layer on our detectors.

DLC layers were deposited by sputtering on silicon wafers covered with aluminum. An easy way to pattern the layers was not found. Lift-off still remains as an option. A low deposition rate inhibits the deposition of thick layers. The

rubber like material did not seem patternable by conventional methods. Also the uniformity after deposition remains unknown. In our next approach we opted for more established technologies. A high resistive layer, made of hydrogenated amorphous silicon (a-Si:H) or silicon rich nitride (SiRN) has been used to cover Medipix2 and Timepix chips. The complete pixel matrix of the chip must be covered with the high resistive layer. The bond pads of the chip are left free of a-Si:H or SiRN to perform the wire bonding. When post-processing single chips a shadow mask was used to cover the bond pads of the chip. When doing complete wafer post-processing a blanket deposition is performed over the wafer. The material is patterned to etch the high resistive layer from the bond pads.

Besides quenching the spark, the a-Si:H or SiRN layer (named anti spark layer) also prevents the evaporation of the thin metal input pads on the CMOS anode chip, due to the spark plasma. Charge from an avalanche, being the result of "normal" single electrons, will arrive and stay on the spark protection layer facing the pixel input pad. A large fraction of this surface charge is seen by capacitive coupling by the pixel input pads.

## 4.2 a-Si:H deposition

Hydrogenated amorphous silicon (a-Si:H) is commonly used in MEMS applications. Low stress a-Si:H structures can be produced. The material is also used for masking; for example in the deep wet etching of glass [88]. In the field of photovoltaics a-Si:H is widely employed in thin film solar cells [89]. Active devices can also be fabricated in a-Si:H. Thin film transistors have been reported [5].

The material is typically deposited at low temperature using Plasma Enhanced Chemical Vapor Deposition (PECVD). The deposition temperature is around 300 °C. The low temperature budget makes it compatible with many post-processing applications. The deposition of the a-Si:H is performed at the Institute of Microtechnology of the University of Neuchatel. It is done using Very High Frequency plasma enhanced chemical vapor deposition (VHF PECVD) at 70 MHz. The temperature of the substrate reaches a maximum of 200 °C. This deposition temperature is compatible with conventional CMOS processing, and plasmas at relatively low bias voltage are employed. This process can thus be included in a wafer scale post-processing sequence on CMOS pixel wafers.

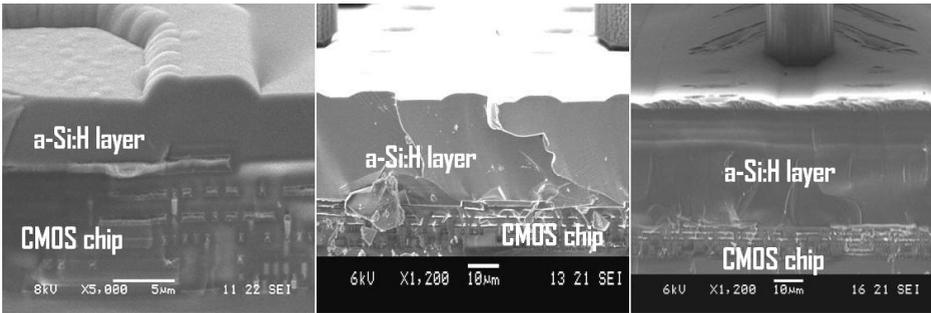
The process is optimized for intrinsic layer deposition at relatively high rates, as used for a-Si:H thick diode deposition [90]. A deposition rate of  $\sim 100$  nm/min. was obtained with a hydrogen dilution of silane ( $[H_2]/[SiH_4] = 0.35$ ). The specific resistivity of the deposited layer (as grown on glass substrate) is around  $10^{11}$   $\Omega$ .cm,

weakly depending on the film thickness and substrate. Doping of the layers is possible to obtain lower resistivities. Stress free layers are obtained.

For the a-Si:H patterning, in the case of single chip processing a lift-off method is preferred. For this purpose, a masking ink is manually deposited over the regions that must be protected during the a-Si:H deposition, particularly the I/O bond pads of the chip. After deposition, the mask is stripped in acetone and the pads of the chip remain free of a-Si:H.

This patterning technique is suitable for large feature sizes but standard photolithography can be applied if smaller contour definitions are required. In this case the a-Si:H is patterned using dry etching in a SF<sub>6</sub>/O<sub>2</sub> plasma.

Several thicknesses of a-Si:H ranging from 3  $\mu\text{m}$  to 30  $\mu\text{m}$  have been deposited on top of Medipix and Timepix chips. Depending on the gas mixture used and the maximum grid voltage applied, a different minimum anti spark layer thickness is needed to protect the chips. Figure 4.5 shows SEM pictures of Medipix chips with three different thicknesses of a-Si:H deposited on top.



**Figure 4.5:** Cross section SEM picture of three Medipix chips covered with different thicknesses of a-Si; 3  $\mu\text{m}$  (left), 20  $\mu\text{m}$  (center) and 30  $\mu\text{m}$  (right).

Even in the case of a 30  $\mu\text{m}$  thick a-Si:H layer, the topography on top of the wafer did not represent a problem for further processing; in particular the spin coating of the SU-8 layer. An homogeneous layer could be achieved with no detriment for the rest of the processing.

## 4.3 SiRN deposition

Stoichiometric  $\text{Si}_3\text{N}_4$  is commonly used in the semiconductor industry. It finds application as passivation layer, interlayer or isolation (LOCOS, deep trench and shallow trench isolation) [91]. Non stoichiometric silicon-rich  $\text{Si}_x\text{N}_y$  (SiRN) is also used in MEMS [92], X-ray masks [93] and RF applications [47] to obtain low stress layers. In both cases the material is typically deposited by LPCVD (low pressure chemical vapor deposition) at a temperature between 700 °C and 900 °C. Using this deposition technique a very good film quality is obtained.

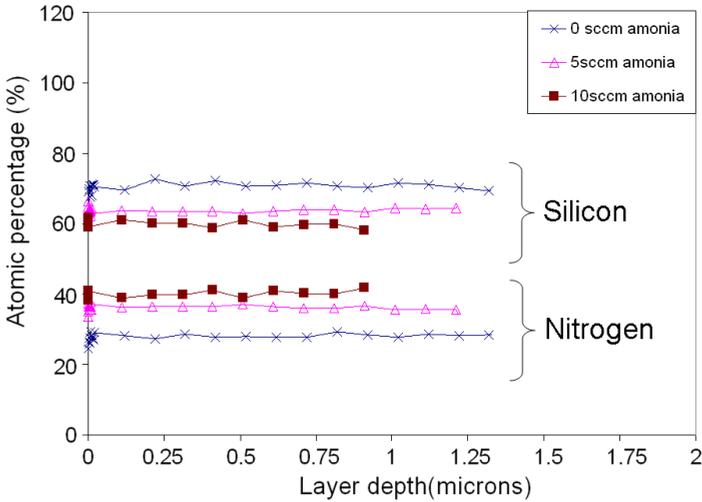
The concentration of silicon and nitride can be tuned to obtain a low stress film [94]. Recently SiRN suspended structures fabricated by PECVD (plasma enhanced chemical vapor deposition) have been shown [95]. The process parameters can be controlled to produce low stress films. The PECVD technique allows to deposit layers at lower temperature than LPCVD. Deposition can be done at temperatures well below 400 °C. This temperature is compatible with CMOS post-processing. PECVD was chosen to deposit silicon rich nitride over the Timepix chips.

The SiRN deposition is done in the MESA+ facilities by PECVD at 13.56 MHz. The pressure inside the chamber was 1000 mTorr. The deposition was done at 300 °C. Silane and ammonia react inside the chamber to form  $\text{Si}_x\text{N}_y$  at the wafer surface. The silicon content in the material can be controlled by changing the ammonia to silane flow ratio. A deposition rate of 70 nm per minute can be achieved. For single chip processing a shadow mask was used to cover the bond pads of the chips and allow deposition in the rest of the areas. Figure 4.6 shows variations in the silicon concentration in the material for different ammonia flows. The silane flow was kept constant. As the silane is diluted in nitrogen (98%), even for no ammonia flow still there will be nitrogen in the material.

The deposition of the SiRN layers was performed in steps of 30 minutes to minimize the time the chips remain continuously at high temperature. The time and temperature chosen for the deposition are common in industry [96]. Figure 4.7 shows a layer of SiRN deposited on top of a Timepix chip in five steps; those steps are clearly seen as an interface oxide is formed after every deposition.

Among all the post-processing steps of our fabrication process the deposition of SiRN by PECVD is the one that presents the highest risk for the CMOS chips. It involves high temperature, the presence of plasmas and induced stress by the thick deposited layer; factors that could induce damage to the CMOS chips [14].

To assess any induced damage during this process, seven Timepix chips were tested before and after the PECVD deposition. For chip C09-W0096 a layer stack of 1  $\mu\text{m}$   $\text{SiO}_2$  and 100 nm  $\text{Si}_3\text{N}_4$  was deposited. For the rest of the chips



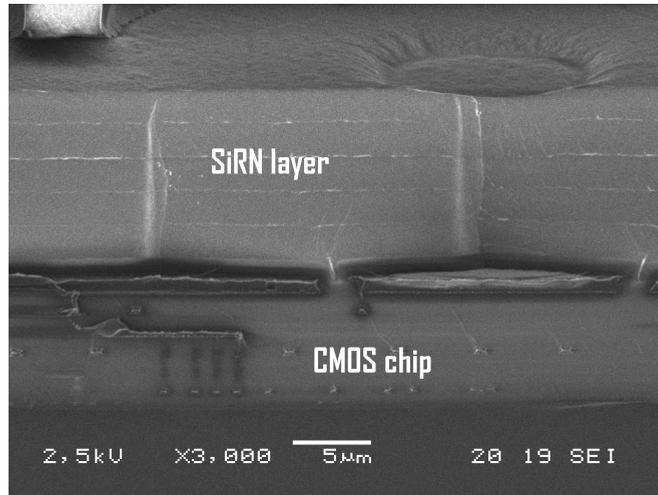
**Figure 4.6:** Silicon and nitrogen concentration as a function of the layer depth for three different ammonia flow during the PECVD deposition. Concentration measurements were done by XPS.

9  $\mu\text{m}$  SiRN were deposited. Pixelman software [97] is used for the testing of the Timepix chips. During the testing the number of inactive columns in the chip is counted. Inactive columns are columns that do not respond during the testing. Therefore those columns will not be available for detection during operation of the detector. In a 200 mm Timepix wafer most of the chips have between zero and two inactive columns. Also the behavior of the digital to analog converters (DACs) [98] is tested. The DACs must have a smooth and monotonous behavior.

Table 4.1 shows the number of inactive columns in those Timepix chips before and after the PECVD deposition. The number of inactive columns did not increase. Only for chip G01\_W0013 one more inactive column appeared. The DAC's performance was not modified either.

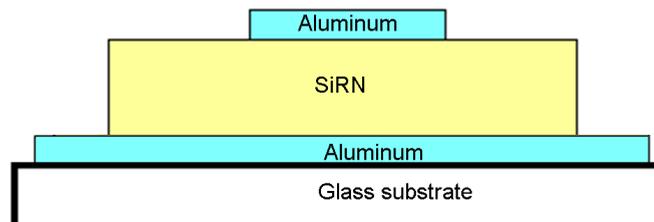
## 4.4 Electrical characterization of the SiRN

To determine the dielectric constant of the SiRN, metal-SiRN-metal test capacitors were built on a glass substrate. Sputtered aluminum 1  $\mu\text{m}$  thick was used



**Figure 4.7:** Cross section SEM picture of a Timepix chip pixel covered with SiRN deposited in five steps, the interface between every layer is clearly seen. Probably an oxide is formed at the interface.

for the bottom electrode. For the top electrode sputtered aluminum 500 nm thick was employed. A  $1.1 \mu\text{m}$  thick SiRN layer was deposited in between the metal electrodes. Capacitors having 0.3 mm, 0.5 mm, 0.7 mm, 1 mm, 1.2 mm, 1.5 mm, 2 mm and 3 mm diameter were fabricated. Figure 4.8 shows an schematic view of a test capacitor.



**Figure 4.8:** Schematic cross section view of a test capacitor.

Chip id	Bad columns before PECVD		Bad columns after PECVD	
	Digital test	Analog test	Digital test	Analog test
B07_W0013	1	1	1	1
B08_W0013	1	1	1	1
I02_W0013	1	1	1	1
G01_W0013	2	2	2	<b>3</b>
I10_W0013	2	2	2	2
I09_W0013	1	2	1	2
C09_W0096	20	20	20	20

**Table 4.1:** Number of inactive columns for several Timepix chips before and after the PECVD deposition.

The capacitance at 0 volts and 100 kHz was measured for the different test capacitors. A Karl Suss PM8 probe station connected to a Keithley 4200 semiconductor characterization system was employed for the measurements. Since the thickness and area of the capacitors are known; it is possible to extract the dielectric constant of the material from the measured capacitance. For a SiRN layer with a 70% silicon content a dielectric constant of 8.7 is obtained. For a SiRN layer with a 60% silicon content a dielectric constant of 6.5 is obtained.

## 4.5 Spark tests

Different thicknesses of a-Si:H and SiRN were deposited on dummy substrates and real CMOS chips. The samples were mounted in a chamber and flushed with a common gas mixture. Sparks were intentionally produced. The protected CMOS chips were also operated in long term experiments under normal biasing conditions. Experimental results are shown in the following sections.

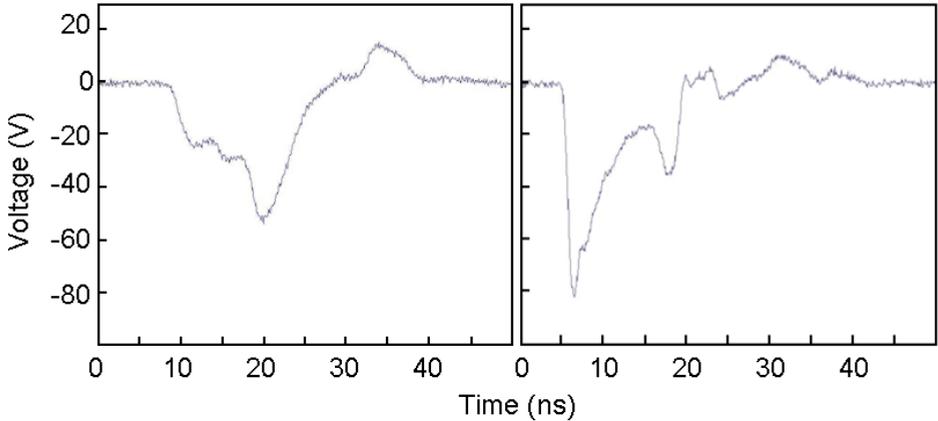
### 4.5.1 Tests on dummy substrates

4-inch silicon wafers containing thirteen  $16 \times 16 \text{ mm}^2$  aluminum anodes were fabricated. On each wafer, eleven anodes were covered with  $3 \mu\text{m}$  a-Si:H. The two remaining anodes were left uncovered for signal comparison purposes. Finally, the wafers were diced, obtaining individual anodes. Micromegas foils were placed on those anodes.

The assembled devices were placed inside the measuring chamber [99], [62].

The chamber was flushed with He/*i*C<sub>4</sub>H<sub>10</sub> (80/20). A container with <sup>232</sup>Thorium was placed in the gas system upstream of the chamber [25]. <sup>232</sup>Thorium decays to <sup>220</sup>Radon which decays through <sup>216</sup>Po to <sup>212</sup>Pb emitting two alpha particles of a few MeV separated by 0.15 seconds.

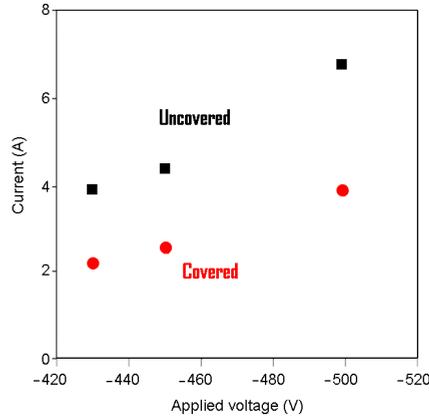
Proportional signals from the alpha particles, measured directly with an oscilloscope connected to the grid, were clearly seen. Figure 4.9 shows spark signals on covered and uncovered anodes at a grid voltage of -490 volts. The signals show a clear difference in the discharge process between the covered and the uncovered anode. The shown signals are representative of hundreds of signals recorded in this manner. The discharge plot in the case of covered anodes has relatively smooth edges and slopes. In the case of the uncovered anodes the discharge plot has a step leading edge.



**Figure 4.9:** Pulse amplitude of discharges on dummy substrates. A discharge on a covered anode (left) and in an uncovered anode (right). Measurements done by M. Fransen.

The current of the discharge was also measured for different grid voltages. As shown in figure 4.10 the current in protected anodes is lower than in unprotected anodes. Also using protected anodes higher gains could be achieved before sparks appear than when using unprotected anodes.

Another way to assess if the resistive layer provides protection against discharges is to measure the detector gain as a function of the grid voltage. The maximum gain that can be reached before sparks appear is determined. Higher



**Figure 4.10:** Discharge peak current for covered and uncovered anodes at different grid voltages. A reduction in the discharge current is obtained when using a covered anode. Measurements done by M. Fransen.

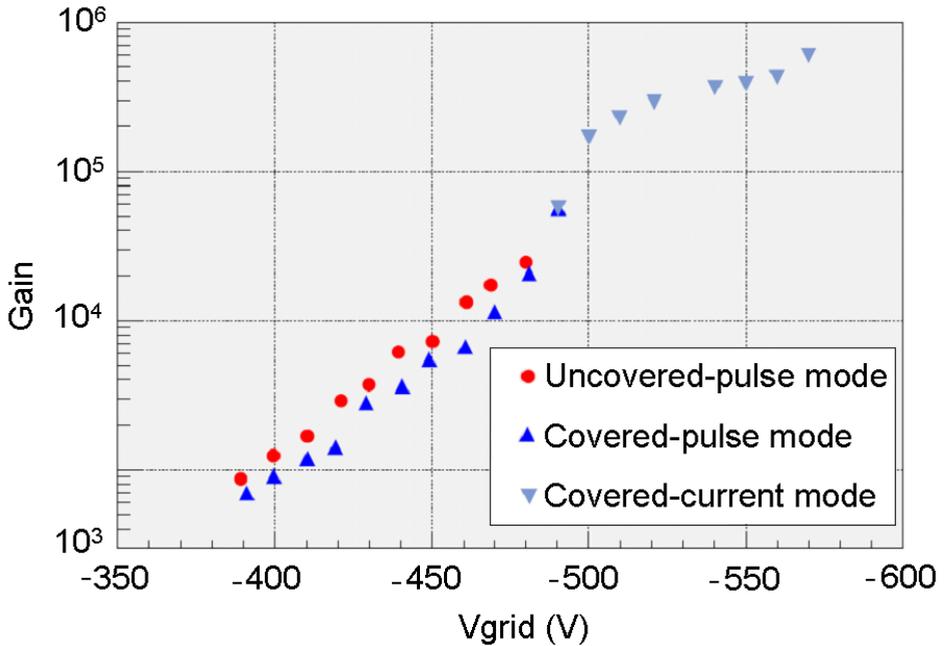
gains are expected for detectors with covered anodes compared with detectors having uncovered anodes.

The gain of detectors with covered and uncovered anodes was measured using an  $^{55}\text{Fe}$  source. Signals from both detectors were amplified and recorded on a digital scope. The currents drawn by the Micromegas meshes were measured too. Figure 4.11 shows the gain curves for both detectors.

The gain curve of the uncovered detector was measured from the  $^{55}\text{Fe}$  pulse area. The gain was measured for grid voltages from -390 V to -480 V. Above -480 V the spark rate becomes too high to operate the detector. Over this range of gain, the current is too small to be recorded accurately.

The gain of the detector with a covered anode was measured. Up to -490 V the  $^{55}\text{Fe}$  pulse area method was employed to determine the gain. No sparks were observed at this stage and the grid voltage could be increased further. The current was enough to allow an accurate current measurement. At -490 V the amplifier started to saturate. Therefore, the gain at higher grid voltages was calculated by converting current into gain. At -500 V the gain is  $170 \cdot 10^3$ . A plateau is reached because of the voltage drop across the resistors in series with the grid. The grid voltage could be decreased up to -570 V and still no sparks were observed. At this voltage, the gain was in the order of  $0.7 \cdot 10^6$ . Below -570 V a destructive spark

occurred that burnt one pillar of the Micromegas mesh. A conductive path from grid to anode was created; what made the detector not functional anymore. The a-Si:H layer was also severely damaged as observed with an optical microscope.



is related to the amount of primary charge released in the conversion gap.

We first operated a TimePix chip with a 3  $\mu\text{m}$  layer of a-Si:H, equipped with a Micromegas in a He/ $i\text{C}_4\text{H}_{10}$  (80/20) gas mixture. The gas gain was adjusted to approximately 5000. During two months cosmic ray events and other types of radiation were recorded. After changing to an Ar/ $i\text{C}_4\text{H}_{10}$  (80/20) mixture, the TimePix chip broke within 8 hours of operation. Visual inspection of the chip surface showed no visible damage like evaporated aluminum or  $\text{Si}_3\text{N}_4$ , as was the case before in naked chips. Apparently, the chip suffered internal damage due to a too large charge injected into one or more pixel input pads.

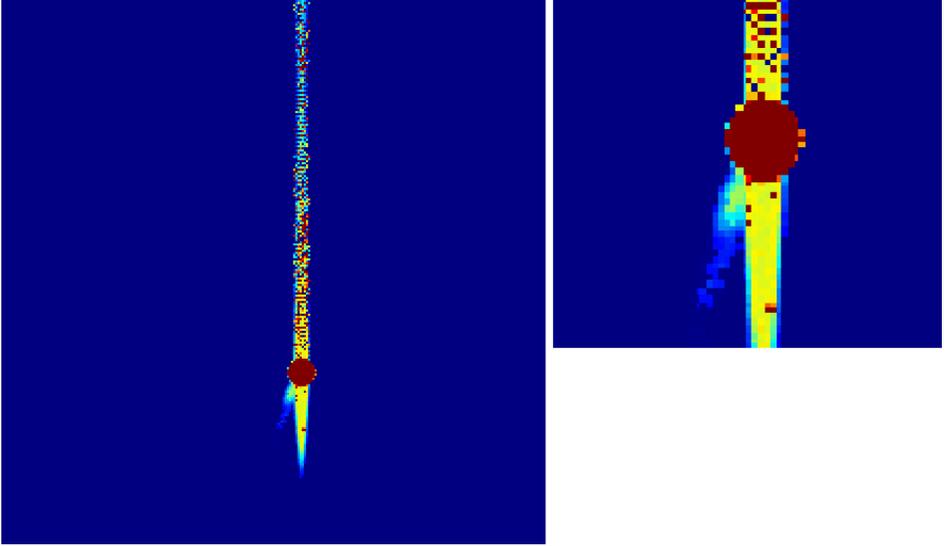
It was decided to cover chips with a thicker layer. This would quench the discharges in an earlier stage. In addition, all induced charge signals appearing at the pixel input pads are somewhat reduced due to the larger distance between the avalanche charge and the pixel input pad. It was realized that charge dilution, as a result of charge spread, would be unavoidable if the thickness of the protection layer is in the order of the pixel input pad. For this reason we chose a new layer thickness of 20  $\mu\text{m}$ . An Ar/ $i\text{C}_4\text{H}_{10}$  (80/20) gas mixture was used. High density primary ionization events were obtained from induced alpha particles. Again the alpha particles were produced from the decay of  $^{232}\text{Thorium}$ .

In about 1% of the alpha events, the proportional signal develops into a discharge. The probability for this is clearly higher for alpha particles with a direction perpendicular to the chip. An example is shown in figure 4.12: where the alpha enters the grid, the discharge occurs, seen in the figure as a red circle. Some 150 pixels in the area receive a large coincident charge signal and are activated. As a result, the local values of supply voltage and threshold references are disturbed. Since these are common within pixel columns, many pixels above and below the discharge area are affected. This does not harm the functionality of the chip.

With a layer of 20  $\mu\text{m}$ , the chips do not only keep functioning: discharges can actually be observed. From this data we conclude that chips, protected with a 20  $\mu\text{m}$  a-Si:H layer, are spark-proof.

### 4.5.3 SiRN protection layers on CMOS chips

To assess the spark protection provided by the SiRN a 13.2  $\mu\text{m}$  thick layer was deposited on a Timepix chip. A Micromegas foil was framed over the chip. The chip was placed in a chamber flushing Ar/ $i\text{C}_4\text{H}_{10}$  80/20. More than -520 volts were applied to the Micromegas foil and the Timepix chip kept functioning normally. Sparks were observed in the chip pixel matrix, as in figure 4.13. The diameter of the spark event seems to be smaller than in the case of a-Si:H. Tracks of cosmic rays were recorded using this chamber. We confirm the normal operation



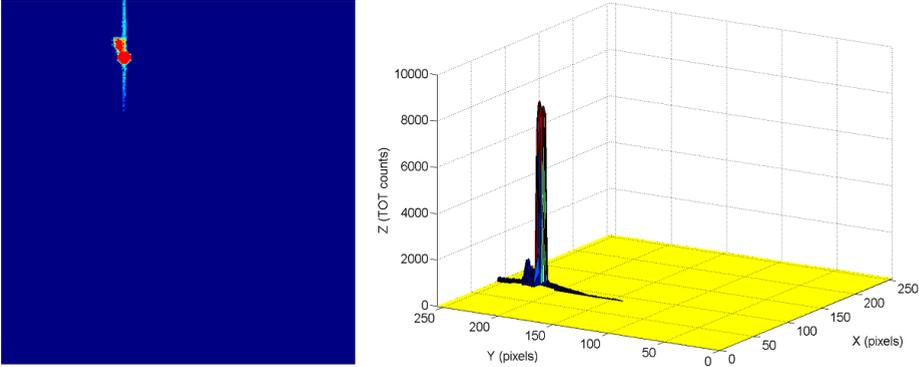
**Figure 4.12:** Left: Typical image of a discharge event in a Timepix chip protected with  $20\ \mu\text{m}$  a-Si:H. The discharge is seen as a red circle. The alpha particle triggering the spark is observed entering the pixel matrix from the bottom left side of the discharge. The pixels activated in the vertical line are due to the disturbance of supply voltage and threshold references. Right: Detail of the spark event.

of the device. Very high voltages were applied without damaging the chip. This SiRN layer provides high spark quenching power. Therefore we believe thinner layers will still provide protection enough against the sparks at normal operating voltages.

When using a-Si, all the pixels involved in a spark event are in overflow. When using SiRN pixels are not in overflow. It is possible to distinguish different values in the spark event. The spark has a tube-like shape with a nearly flat top.

## 4.6 Results and discussion

We have deposited different layers of a-Si:H and SiRN on CMOS chips. They have been exposed to discharges. Also long term normal operation has been



**Figure 4.13:** Raw image of a typical image of a discharge event in a Timepix chip protected with  $13.2 \mu\text{m}$  SiRN (left). The same discharge reconstructed in three dimensions (right).

evaluated. Table 4.2 summarizes the obtained results. The spark insensitivity of CMOS chips can only be proved by exposing a large number of detectors during a long time to a lot of discharges. This experiment was not yet carried out. Although our work as presented in the previous sections cannot be considered a systematic study some conclusions can be drawn after our experiments.

- Helium based mixtures are less prone to sparks than argon based mixtures. We assume this is due to the lower total ionization density of helium compared to argon. For the same total avalanche charge the spark probability is the same [77]. Also the tails of the charge distribution of minimum ionizing particles in helium is shorter than in other gas mixtures. This leads to lower spark probability [100].
- From RPC signals and our own measurements we know that a resistive layer reduces the electric field and quenches the discharge after a certain fraction of the energy is dissipated. We do not know the discharge mechanism such that we could predict this fraction.
- After optical inspection of SiRN and a-Si:H protection layers after many discharges, surface material evaporation nor melting has been observed. We conclude that the energy, dissipated in the discharge, does not heat up the surface such that evaporation or melting takes place.

- After exposing Timepix chips during a long time to discharges the chips maintained their original response. We conclude that the maximum charge, induced in a pixel, due to a typical discharge, does not exceed the maximum tolerable signal charge on the pixel input pad.
- The thicker the protection layer the better the chip is protected against discharges.
- A 20  $\mu\text{m}$  thick a-Si:H layer provides enough protection for our typical working point (gas mixture, geometry, applied voltage). Thinner layers do not protect the chips in all cases.
- An 11  $\mu\text{m}$  thick SiRN layer is effective to protect the Timepix chips for our typical working point (gas mixture, geometry, applied voltage).
- With the present knowledge we expect that the CMOS chips will be sufficiently protected against naturally occurring sparks. Since details about the discharge development are not known and variations in material parameters can not be excluded, there is no guarantee. In addition, other discharge processes may occur of which we are not aware of.

With the use of an adequate thickness of a-Si:H or SiRN, depending on the gas mixture, the time to failure of the chips is considerably increased from hours to months.

Layer	gas mixture	test voltage	time of failure
3 $\mu\text{m}$ a-Si	He/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	~ -420 V	> 2 months
3 $\mu\text{m}$ a-Si	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	~ -420 V	8 hours
15 $\mu\text{m}$ a-Si	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (95/5)	~ -350 V	> 4 months
15 $\mu\text{m}$ a-Si	Xe/CO <sub>2</sub> (80/20)	-490 V	2 hours
20 $\mu\text{m}$ a-Si	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	~ -420 V	> 8 months
20 $\mu\text{m}$ a-Si	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	provoked discharges	> 1 day
13.2 $\mu\text{m}$ SiRN	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	Provoked discharges	> 1day
13.2 $\mu\text{m}$ SiRN	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	~ -420 V	> 2 months
11 $\mu\text{m}$ SiRN	Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	Twingrid -640 V on the top grid. -200 V on bottom grid	> 2 months

**Table 4.2:** Summary of discharge tests on several chips for different protection layer thicknesses and operating conditions.



# Experimental results with InGrid and GEMGrid

This chapter presents measurements performed with InGrid and GEMGrid structures. These include single electron detection with high efficiency, three dimensional track reconstruction and X-ray imaging.

The breakdown voltage of InGrid and GEMGrid was measured; this gives a comparison between Micromegas-like and GEM-like structures processed in the same conditions, using same materials and having same dimensions. A beam test was performed at the PS/T9 beam line at CERN with InGrid devices in several gas mixtures.

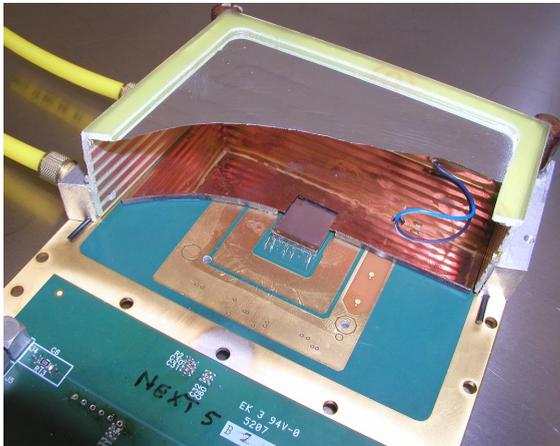
## 5.1 Measurement setup

For testing of the InGrid and GEMGrid devices a small drift chamber was built. This chamber consists of a printed circuit board on which the chip was mounted and wire bonded. A 3 cm gap field cage is used as cover for the chamber to seal a region around the chip. At the same time, the field cage creates a uniform drift field. For some experiments a 10 cm gap field cage was used. A guard ring electrode 1 mm higher than the chip was placed closely around the device. The voltage applied to the guard ring is some tens of volts higher than the grid voltage. This ensures an uniform electric field in the region close to the chip. Feedthroughs made in the field cage allow flushing the gas into the chamber. A

picture of an assembled Timepix/Ingrid chamber is shown in figure 5.1.

The Timepix chip is fabricated in  $0.25\ \mu\text{m}$  CMOS technology. It contains  $256 \times 256$  pixels arranged in an area of about  $14\ \text{mm} \times 14\ \text{mm}$ . It has three detection modes: it provides, during a preset acquisition time window, either the number of electron avalanches recorded at each pixel (Medipix mode), the arrival time of an avalanche (Timepix mode) or the charge contained in an avalanche (TOT mode). To be detectable, the charge induced by an avalanche at a pixel input should be higher than the pixel threshold; set around 800 electrons.

The output of the printed circuit board is connected through a MUROS2 [101] interface to a computer, to read out the output signals of the chip. Pixelman [97] software provides the interface to collect the data.



**Figure 5.1:** View of the assembled Timepix/InGrid chamber. A chip in the center, wire bonded to the PCB, can be seen through a cut in the field cage.

## 5.2 InGrid vs GEMGrid

In chapter 2 the fabrication process for InGrid and GEMGrid structures was presented. The same dimensions and materials are used for Micromegas-like and GEM-like structures. Therefore the two structures can be directly compared. In the following sections the breakdown voltage of both structures as well as the single electron efficiency are studied.

### 5.2.1 Breakdown voltage

To compare the high voltage capability of InGrid and GEMGrid structures, in several gases, we measured at what voltage sparks start to appear. In all cases the critical spark voltage is significantly lower for the GEM-like structure with non recessed SU-8 walls. This is summarized in table 5.1. As a consequence, the integrated GEM-like structure reaches significantly lower gain than the integrated Micromegas-like structure.

At this lower gain minimum ionizing particle detection was not possible. The difference was assumed to be a direct result of the recessed aluminum; the aluminum holes having a larger diameter than the SU-8 holes. In this case the dielectric can charge up. Also an intense electric field can be found near the surface of the insulator, leading to sparks. This problem is not present in Micromegas-like structures as the pillars are always well hidden under the metal electrode.

	GEM-like	Micromegas-like
He/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	-420 volts	-470 volts
Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (95/5)	-280 volts	-360 volts
Ar/ <i>i</i> C <sub>4</sub> H <sub>10</sub> (80/20)	-380 volts	-470 volts
Ar/CO <sub>2</sub> (70/30)	-315 volts	-480 volts

**Table 5.1:** Spark limit for GEM-like and Micromegas-like structures.

It was believed the diameter mismatch is the root cause of the relatively low breakdown voltage in the GEM-like structure. To verify this, a GEMGrid with recessed SU-8 walls was fabricated and tested. The holes in the insulator are 46  $\mu\text{m}$  in diameter while the holes in the metal are 30  $\mu\text{m}$  in diameter. SEM pictures of GEMGrid structures with recessed and non recessed SU-8 can be found in chapter 2. In Ar/*i*C<sub>4</sub>H<sub>10</sub> (95/5), it was established that this GEM-like structure maintains -350 volts before sparking, therefore closing in on the Micromegas performance.

### 5.2.2 Single electron counting

In this section we present single electron counting measurements. Timepix chips equipped both with InGrid and GEMGrid were used. The devices were irradiated with an <sup>55</sup>Fe source. The measurements were performed using a 10 cm gap field cage and Ar/*i*C<sub>4</sub>H<sub>10</sub> (95/5) gas mixture. The electron transverse diffusion in this gas mixture is enough to spread the primary charge of an <sup>55</sup>Fe

conversion over the chip surface. The number of activated pixels is proportional to the number of primary electrons. By summing up the number of hit pixels in every  $^{55}\text{Fe}$  cloud the spectrum can be reconstructed. Figure 5.2 shows a typical  $^{55}\text{Fe}$  spectrum obtained with InGrid (top) and GEMGrid (bottom). Good energy resolution of 12.6% FWHM is obtained for both devices. The peak position is at higher value for InGrid than for GEMGrid. This indicates a better single electron detection for InGrid.

To determine the single electron efficiency, the  $^{55}\text{Fe}$  spectrum was reconstructed for several grid voltages. The number of detected electrons divided by the expected primary charge gives the single electron efficiency.

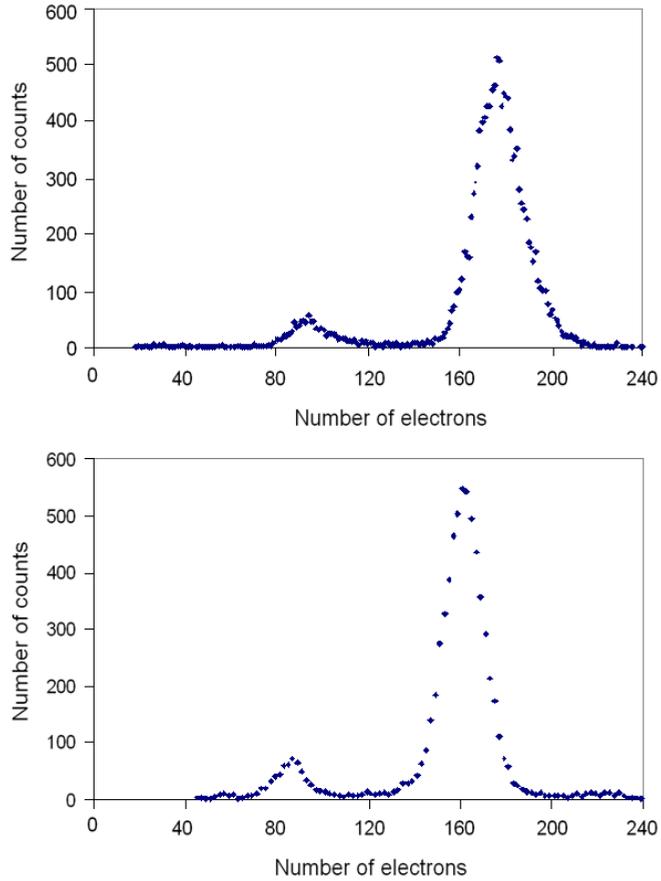
Counting the number of activated pixels can be problematic if electrons are not separated enough. If two electrons are close together they activate neighbouring pixels. Due to the charge sharing induced by the anti-spark layer [62], [102]; it is not always possible to discriminate if two neighbour pixels were produced by two electrons or by charge sharing effects. Also if two electrons arrive to the same grid hole they will only activate one pixel. For the previous reasons it is desirable to have few hits to count. The escape peak contains half the number of electrons than the photo peak.

Therefore, the number of detected electrons in the escape peak of the  $^{55}\text{Fe}$  spectrum were counted instead of the main peak. As primary charge 110 electrons were assumed [103]. The variation of the single electron efficiency with the grid voltage could be measured by this method. Figure 5.3 shows the single electron detection efficiency of the InGrid and GEMGrid as a function of voltage. The detection efficiency for InGrid devices is about 100%. A 85% detection efficiency is obtained with GEMGrid devices before reaching the spark limit.

### 5.2.3 Gain of GEMGrid

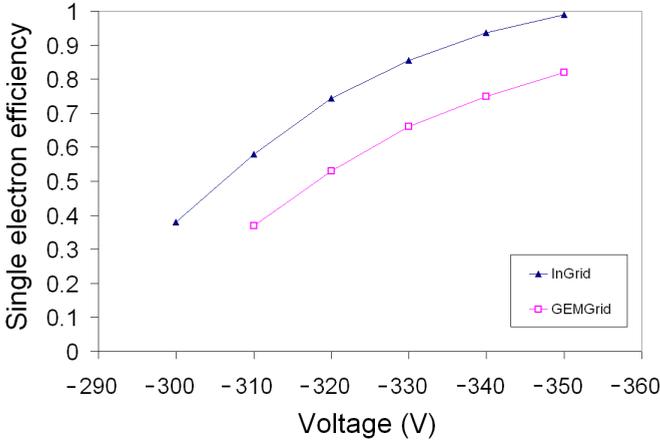
The gas gain of a GEMGrid device was measured using  $\text{He}/i\text{C}_4\text{H}_{10}$  (77/23) gas mixture. The device was irradiated with a collimated  $^{55}\text{Fe}$  source. The maximum pulse height at the grid was measured. In this gas mixture the  $^{55}\text{Fe}$  spectrum contains a main peak and a Compton background. To deduce the gain from the maximum pulse height it was assumed that in  $\text{He}/i\text{C}_4\text{H}_{10}$  (77/23) an  $^{55}\text{Fe}$  event produces 160 primary electrons on average in the main peak [103].

The results are shown in figure 5.4. Stable operation at gains exceeding  $10^4$  has been achieved, indicating that in this gas mixture the detector can reach an even higher single-electron efficiency than quantified before. We must point out that the grid used in InGrid structures had  $40\ \mu\text{m}$  hole diameter. The GEMGrid devices had a grid with  $30\ \mu\text{m}$  hole diameter. With this dimensions collection



**Figure 5.2:** Detector performance illustrated from X-ray radiation response, operating in Ar/ $i$ C<sub>4</sub>H<sub>10</sub> (95/5) at -335 volts (top, InGrid) and -340 volts (bottom, GEMGrid) on the grid. The histograms show a count spectrum of <sup>55</sup>Fe radioactive decays reconstructed from summing up the number of single electron avalanches.

efficiency of Ingrid devices would be probably better than for GEMGrid devices [62].



**Figure 5.3:** Single electron efficiency as a function of the grid voltage. Values are deduced from the number of electrons in the escape peak of the  $^{55}\text{Fe}$  spectrum for InGrid (top) and GEMGrid (bottom).

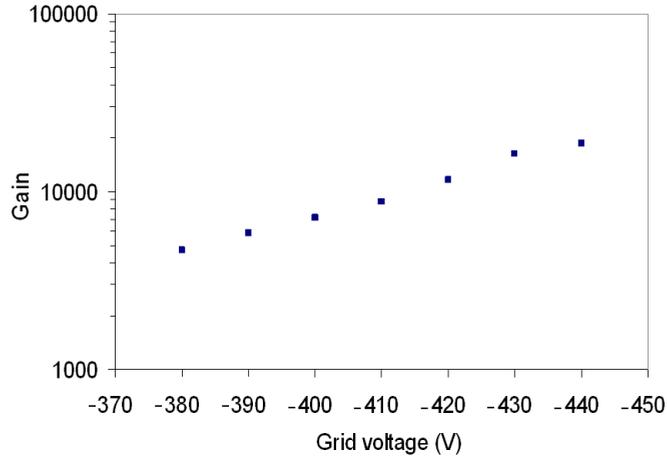
## 5.3 Radiation imaging

In this section we present some of the images taken with InGrid and GEMGrid devices. Track reconstruction and X-ray imaging can be performed. The several images shown prove the device can detect minimum ionizing particles, and a high single electron efficiency is achieved.

### 5.3.1 X-ray imaging

As a first test the InGrid device was irradiated with 6 keV photons produced by an  $^{55}\text{Fe}$  radioactive source. A typical image with several  $^{55}\text{Fe}$  clouds along the pixel matrix is shown in figure 5.5.

If the exposure time is increased we can obtain a footprint of the grid above the Timepix chip. This integral image of the hits per pixel is shown in figure 5.6 left. We obtained a homogeneous response thanks to the good alignment between the holes of the grid and the pixels of the chip. To quickly illustrate imaging capability, a circular metal nut was placed on top of the chamber, locally absorbing the  $^{55}\text{Fe}$  photons. Figure 5.7 shows the resulting image of the nut using  $\text{He}/i\text{C}_4\text{H}_{10}$  (80/20) as gas mixture. Gas avalanche detectors have been widely used for medical



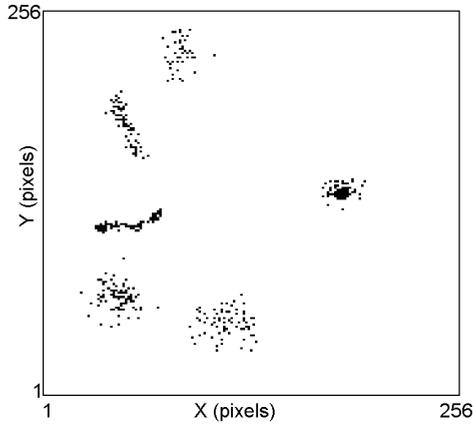
**Figure 5.4:** Measured gas gain vs. grid voltage in a GEMGrid device with 30  $\mu\text{m}$  hole diameter using  $\text{He}/i\text{C}_4\text{H}_{10}$  (77/23) gas mixture.

imaging [104], [105], [106]. To obtain a better image reconstruction the system must be optimized. A gas with small transverse diffusion must be used (e.g. xenon) and high pressure should be applied.

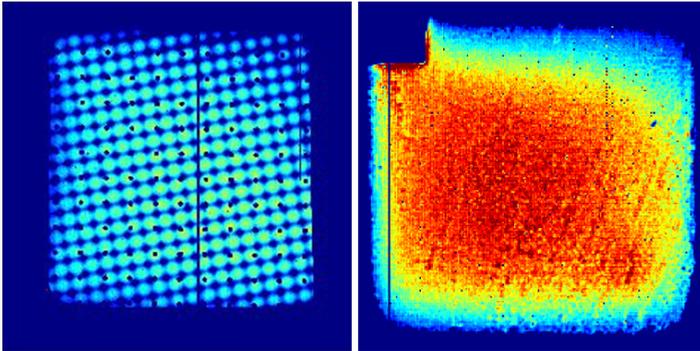
For comparison, figure 5.6 left shows a footprint of a not integrated Micromegas foil. Side areas of the chip are not available for detection due to the Micromegas frame. Pillars lying on top of pixels are seen as dead areas. The different pitch between holes in the Micromegas and pixels in the chip produces inefficient areas because of the Moiré effect. All these drawbacks are overcome when using InGrid.

### 5.3.2 Imaging minimum ionizing particle tracks

With the good single electron detection of InGrid and GEMGrid, tracking of minimum ionizing particles with high efficiency is possible. Figure 5.8 left shows a track of electrons emitted by a  $^{90}\text{Sr}$  source. Three dimensional reconstruction is possible using the drift time information provided by the Timepix chip. A  $\delta$ -ray coming out from the main trajectory is clearly seen. In normal gaseous detectors such  $\delta$ -electrons lead to poor track reconstruction and position resolution. Now with this full 3D information discrimination against  $\delta$ -rays is possible, producing



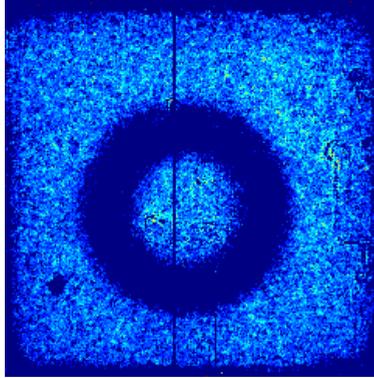
**Figure 5.5:** Raw image obtained with a InGrid/Timepix device after irradiation with  $^{55}\text{Fe}$  in  $\text{He}/i\text{C}_4\text{H}_{10}$  (80/20) and a 3 cm gap field cage. Six  $^{55}\text{Fe}$  clouds with varied diffusion, depending on the conversion point, are observed in the pixel matrix.



**Figure 5.6:** Integral image of hits per pixel after irradiation with  $^{55}\text{Fe}$ . A homogeneous response is observed in the right for an InGrid/Timepix assembly. Moiré effect and unusable areas appear when using a Micromegas/Timepix device (left).

a better track fit.

Devices were also operated in a 0.5 T magnetic field. A track produced by



**Figure 5.7:** Image of a circular nut obtained with the InGrid/Timepix assembly irradiating the device with an  $^{55}\text{Fe}$  source.

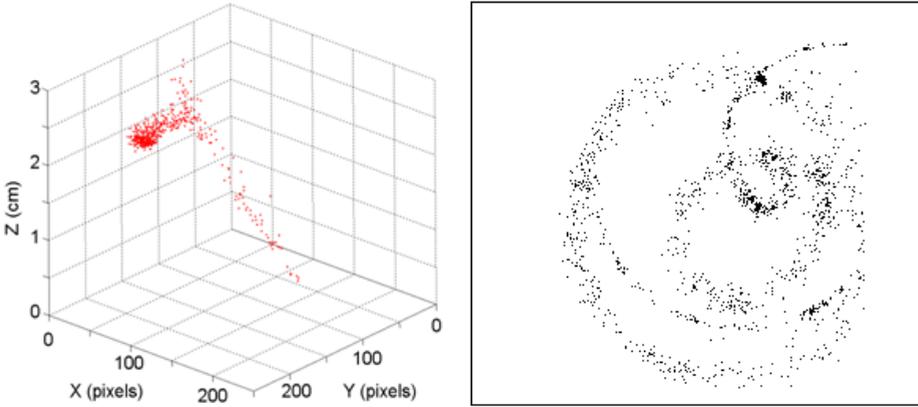
electrons emitted from a  $^{90}\text{Sr}$  source curving in the magnetic field is seen in figure 5.8 right. This information is essential for the measurement of charge and momentum of the incoming particle. Also energy loss measurements can be performed. Several Timepix chips equipped with InGrid and GEMGrid have been continuously operated for several months in argon and helium based gas mixtures while recording cosmic ray events and other types of radiation with stable and unchanged operation.

### 5.3.3 Beam test

One of the key tests of every radiation detector is to assess the performance under beam test conditions. A beam test was performed in May 2008 at the PS/T9 line at CERN [107]. This beam line produces pions and electrons with energies up to 10 GeV. Two Timepix chips with an integrated InGrid were tested in these conditions. One of the chips had a  $15\ \mu\text{m}$  thick a-Si protection layer. The other chip had a  $20\ \mu\text{m}$  thick a-Si layer.

Typically a reference position sensitive detector is used during beam test. Spatial resolution of the tested detector is compared with the one given by the reference position sensitive detector. Unfortunately, we did not have a reference position sensitive detector during the beam test.

The beam test setup is shown in figure 5.9. A chamber having a 17 mm gap field cage is aligned with the beam. The chamber is placed such that the beam

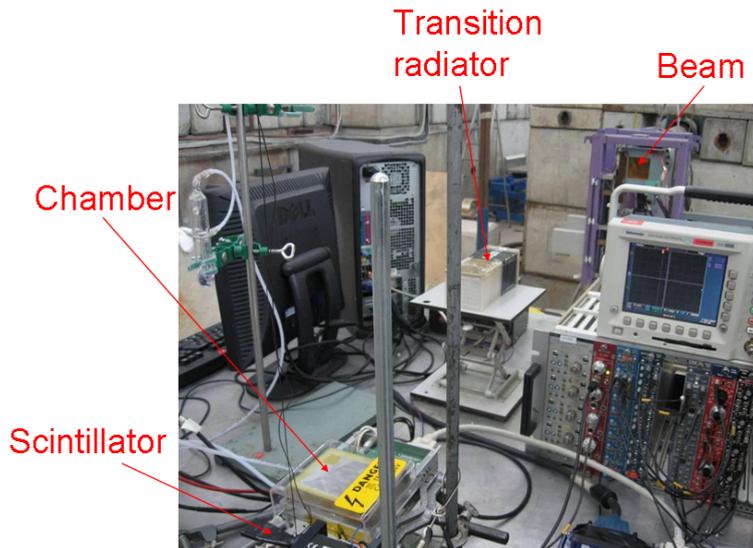


**Figure 5.8:** Typical 3D reconstructed track (left) and 2D track in a 0.5 T magnetic field (right) crossing the detector area produced by electrons emitted by a  $^{90}\text{Sr}$  source.

crosses the field cage. In some data taking runs, beam particles pass parallel to the chip, leaving a long track along the chip surface. In another configuration the chamber is inclined so tracks cross through the chip. A scintillator after the chamber, and aligned with the beam, marks the time when a particle has passed through the chamber.

Four different gas mixtures were used, Xe/CO<sub>2</sub> (70/30), He/*i*C<sub>4</sub>H<sub>10</sub> (80/20), Ar/CO<sub>2</sub> (70/30) and Ar/CF<sub>4</sub>/*i*C<sub>4</sub>H<sub>10</sub> (95/3/2). Figure 5.10 shows typical tracks recorded in those gas mixtures. We notice that more than five tracks can be clearly distinguished in the chip area. Different gas mixtures were employed to study electron diffusion. The preliminary results fit well with the expected values. Ar/CF<sub>4</sub>/*i*C<sub>4</sub>H<sub>10</sub> (95/3/2) in a magnetic field and Xe/CO<sub>2</sub> (70/30) gas mixtures present low transverse diffusion. That makes them suitable to obtain the best spatial resolution.

The devices were tested to see their performance in a transition radiation tracker [108]. For this purpose, a transition radiator was placed close to the chamber and in line with the beam. For a 5 GeV energy the electrons have a Lorentz factor [109] of 10000 and the pions of 36. Therefore electrons are the more likely to create transition radiation. Figure 5.11 shows two electron tracks, with (right) and without (left) transition radiator in front of the chamber. Xe/CO<sub>2</sub> (70/30) was used for the transition radiation measurements. The X-ray photon

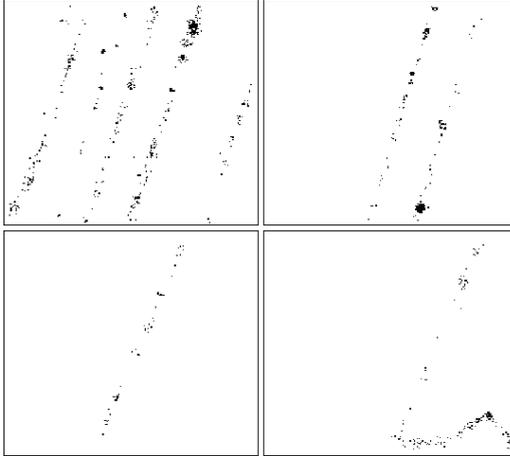


**Figure 5.9:** Beam test setup. A chamber with a 17 mm gap field cage is aligned with the beam. A transition radiator is placed in front of the chamber. A scintillator behind the chamber marks the arrival of a particle.

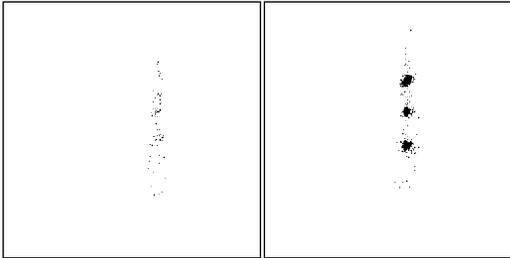
conversions can be clearly seen as dense energy deposits along the track when the transition radiator is placed in front of the chamber. The acquired data are not yet fully analyzed at the time of writing this thesis.

All the previous tracks, measured in various gas mixtures, magnetic field and applied voltages, show an operational fully digitally read-out device. Electrons liberated by charged particles traversing a gas volume can be observed individually. The device provides the information needed to reconstruct the three dimensional trajectory of a charged particle and determine its energy loss in the gas mixture.

Tests with a reference position sensor will be done in the near future to determine the spatial resolution of the sensor. Several detectors will be tiled together. A bigger area is obtained this way and measurements of energy loss can be done more precisely.



**Figure 5.10:** Image of tracks taking during the beam test, from left to right and top to bottom, in Xe/CO<sub>2</sub> (70/30), He/*i*C<sub>4</sub>H<sub>10</sub> (80/20), Ar/CO<sub>2</sub> (70/30) and Ar/CF<sub>4</sub>/*i*C<sub>4</sub>H<sub>10</sub> (95/3/2).



**Figure 5.11:** Image of two tracks produced by 5 GeV electrons crossing the detector area. Left, no transition radiator in front of the chamber. Right, a transition radiator in front of the chamber. Blobs from X-rays conversions along the track are clearly seen.

## 5.4 Conclusions

To conclude this chapter we would like to compare the performance of InGrid detectors with other technologies. Table 5.2, reproduced from reference [108],

summarizes the characteristics of various detectors.

Detector type	Accuracy (rms)	Resolution time	Dead time
Bubble chamber	10-150 $\mu\text{m}$	1 ms	50 ms
Streamer chamber	300 $\mu\text{m}$	2 $\mu\text{s}$	100 ms
Proportional chamber	50-300 $\mu\text{m}$	2 ns	200 ns
Drift chamber	50-300 $\mu\text{m}$	2 ns	100 ns
Scintillator		$\sim 50$ ps	10 ns
Emulsion	1 $\mu\text{m}$		
Liquid Argon Drift	$\sim 175$ -450 $\mu\text{m}$	$\sim 200$ ns	$\sim 200$ $\mu\text{s}$
Gas Micro Strip	30-40 $\mu\text{m}$	10 ns	200 $\mu\text{s}$
RPC	10 $\mu\text{m}$	1-2 ns	
Silicon strip	pitch/(3 to 7)	Electronics	Electronics
Silicon pixel	2 $\mu\text{m}$	Electronics	Electronics

**Table 5.2:** Typical resolutions and dead times of common detectors.

Using a one millimeter drift region, InGrid detectors can have spatial resolution similar to silicon detectors, with a fast response of  $\sim 20$  ns and low occupancy. Also high counting rates can be achieved. InGrid devices could be used as vertex detector. This concept is called GOSSIP (gas on slimmed silicon pixels). Some benefits are present when compared to silicon detectors:

- Less material in the detector.
- No radiation damage of the detector is expected as the gas is exchanged.
- Low power and therefore less cooling is needed.

Ingrid devices are planned to be used in the readout place of Time Projection Chambers (TPC). TPCs using Micromegas or GEMs in the readout plane have already been shown [110], [111]. Using InGrid devices the readout electronics is simplified. The high granularity of the grid is fully exploited when coupled to a readout chip. We are facing the start of the digital TPC. X-ray polarimetry will also benefit when using InGrid devices. The concept has already been shown when coupling a GEM to a CMOS readout chip [112].



# Chapter 6

## Multistage detectors

This chapter deals with the fabrication and properties of multistage Micro Patterned Gaseous Detectors (MPGD). We show the possibility of building a variety of new structures with several metal grids on CMOS chips using wafer post-processing. In these structures a lower spark rate can be achieved by adjustment of the voltage and gap thickness.

### 6.1 Introduction

The use of multistage gaseous detectors has been widely reported. These detectors consist of several amplification stages one on top of another. The primary charge is successively amplified in the different stages. The expected benefits of the multistage configuration include the following:

- Fast signal development, as it will be given by electrons, moving faster than ions.
- Reduced ion back flow.
- Low risk of sparks.

Devices like PIM [113], Micromegem [114], GEM-MIGAS [115], and especially, double or triple GEM have been successfully operated. The multiple GEM configuration can provide high gain with a low risk of sparks [25]; this is a key issue for the safe operation of gaseous detectors. A triple GEM stack coupled to a Timepix

chip has been shown to be operational without chip damage due to sparks and reaching enough gain for minimum ionizing particles detection [116]. But these devices suffer even more severely the problem of misalignment between holes of the device and pixels of the chip.

As a natural continuation of the single stage devices our aim was to build integrated multistage devices on top of CMOS chips using wafer post-processing techniques. The following sections describe a modified fabrication process for the fabrication of multistage devices and show their performance.

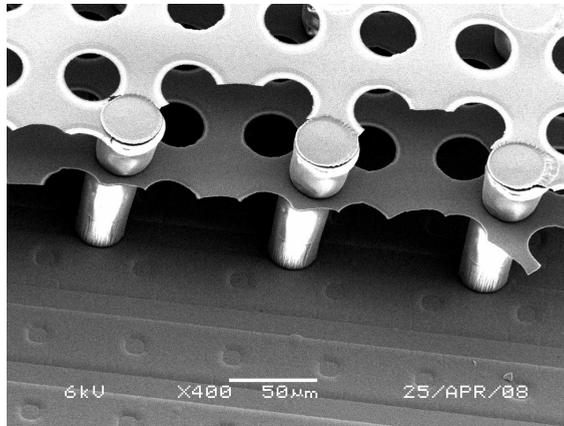
## 6.2 Fabrication process

SU-8 has been reported to be used in MEMS technology to produce multilayer structures. This is done by spin coating a SU-8 layer on top of another previously deposited and exposed SU-8 layer [117], [118], [119]. Inspired by these results, SU-8 seems to be a promising candidate to build upper layers in multistage Micro Patterned Gaseous Detectors. Two designs of multistage detectors were fabricated and tested. In the first design an InGrid structure was placed on top another InGrid structure. In the second design an InGrid structure was built on top of a GEMGrid structure. Figure 6.1 and figure 6.2 show those two types of multilayer structures, generally named as TwinGrid.

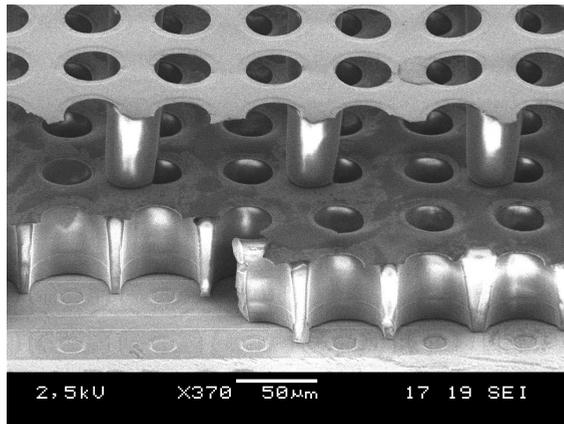
In case the bottom layer of the detector is a GEMGrid, liquid SU-8 was chosen as structural material for the top layer, and it was processed as a standard InGrid. On the contrary, when the bottom layer is an InGrid the use of liquid SU-8 produces undesired results depending on the geometry of the detector. This is due to the fact that to cure the spin coated liquid SU-8 a temperature of 95 °C must be maintained for a certain time; this produces deformation in the layer underneath, due to the SU-8 reflow, which induces an unacceptable deformation in the metal grid. To overcome this effect, the use of SU-8 foil instead of liquid SU-8 for upper stages is preferred.

SU-8 foil is sold in sheets of 12 x 9.5 inches (50 foot rolls are available upon request) of 9  $\mu\text{m}$ , 14  $\mu\text{m}$  and 20  $\mu\text{m}$  thick. Several foils can be stacked one on top of another to obtain thicker layers. SU-8 foils have some advantages over liquid SU-8:

- A reduced number of processing steps.
- A reduced amount of wasted material.
- Edge bead removal is not necessary.



**Figure 6.1:** SEM picture of a TwinGrid structure (InGrid on top of InGrid) on a Timepix chip protected with a-Si. Bottom stage is 50  $\mu\text{m}$  thick. Top stage is 40  $\mu\text{m}$  thick.



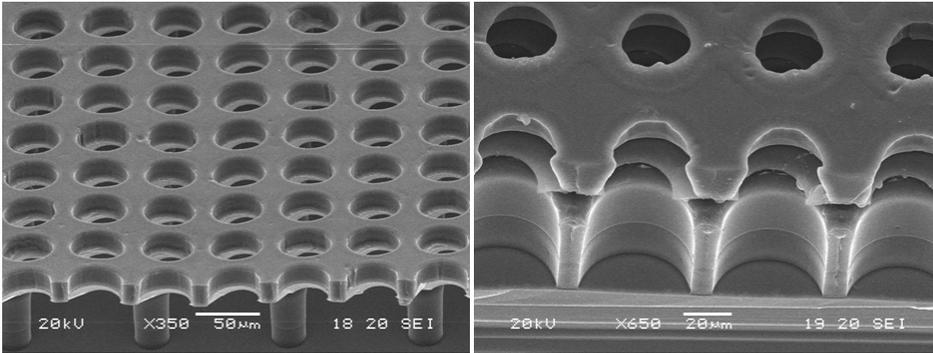
**Figure 6.2:** SEM picture of a TwinGrid structure (InGrid on top of GEMGrid) on a Timepix chip protected with SiRN. Top and bottom stages are 50  $\mu\text{m}$  thick.

The material is not as widely used as liquid SU-8 and at this moment it is only available for sale for engineering trials. No information on SU-8 foils is found in the literature. The fabrication steps for the SU-8 foil part are as follows:

- Lamination of two 20  $\mu\text{m}$  thick SU-8 foils in a hot roller laminator at 70  $^{\circ}\text{C}$ . Foil lamination is performed in two runs. Note that no soft bake is needed.
- Exposure of the resist (34 seconds at 12  $\text{mW}/\text{cm}^2$ , near UV broad band 350 nm-450 nm).
- Post exposure bake of the resist at room temperature overnight.

At present the yield for TwinGrid structures is about 20%; considerably lower than for InGrid and GEMGrid devices. More work should be done to increase the yield before the structures can be fabricated in a semi-industrial process.

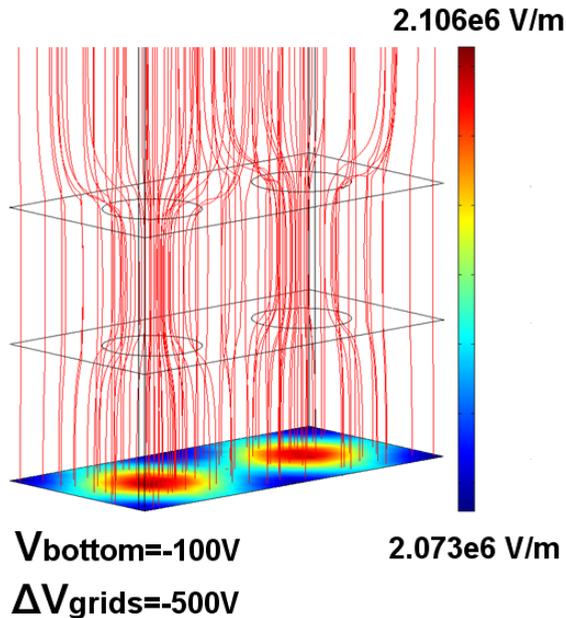
The TwinGrid structures shown in figure 6.1 and figure 6.2 were successfully tested under high voltage conditions and radiation. Two other combinations can be fabricated: one where both the bottom layer and the top layer are GEMGrid type, producing a very robust device from the mechanical point of view, and another one having an InGrid as bottom layer and GEMGrid as top layer, resembling a GEM with a 50  $\mu\text{m}$  extraction gap. SEM pictures of those devices are seen in figure 6.3.



**Figure 6.3:** Left: SEM picture of an GEMGrid on top of InGrid. Right: SEM picture of a GEMGrid on top of GEMGrid. In both cases the lower layer and upper layer are 50  $\mu\text{m}$  thick and 20  $\mu\text{m}$  thick respectively. The upper grid is made with non recessed SU-8.

## 6.3 TwinGrid on Timepix chip

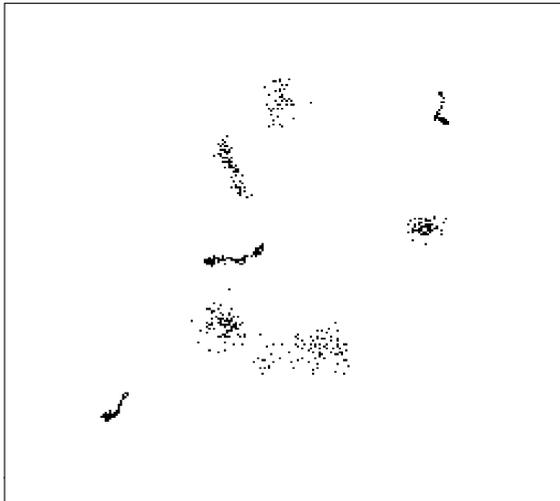
The first goal of the TwinGrid structure was to investigate the possibility to eliminate lethal sparks. This was based on the idea that a reduced electric field facing the chip would reduce spark probability. With our biasing conditions the electric field facing the chip was reduced from typically 100 kV/cm in the normal InGrid to 20 kV/cm in the TwinGrid; although it can still be further decreased. Figure 6.4 shows the simulated electric field of a double grid structure. For the testing of the chips equipped with the TwinGrid structure the same chamber described in chapter 5 was employed.



**Figure 6.4:** Simulated electric field of a TwinGrid structure. Comsol Finite Element Modeling software was employed for the simulation. A reduced electric field of 20 kV/cm facing the bottom surface can be obtained at normal operation conditions.

A Timepix chip without any anti-spark protection layer was equipped with TwinGrid and irradiated with a  $^{55}\text{Fe}$  source. A He/ $i\text{C}_4\text{H}_{10}$  (80/20) gas mixture

was used to minimise the risk of sparks. The device was biased applying -450 volts to the upper grid and -130 volts to the lower grid. Figure 6.5 shows some  $^{55}\text{Fe}$  clouds obtained in this configuration using a 3 cm drift gap field cage. After five hours of operation the chip did not respond anymore, and the noise level could not be controlled with the DACs levels. This was the same problem faced in an early stage when chips equipped with a Micromegas foil were not protected with an anti-spark layer. This leads us to conclude that a spark has caused sudden death and therefore TwinGrids are no panacea against destructive discharges. More tests reducing the electric field in the lower region should be done.



**Figure 6.5:** Image of eight  $^{55}\text{Fe}$  clouds spread over the chip area recorded with a 3 cm drift gap field cage. The area of the picture corresponds to the full area of the Timepix chip

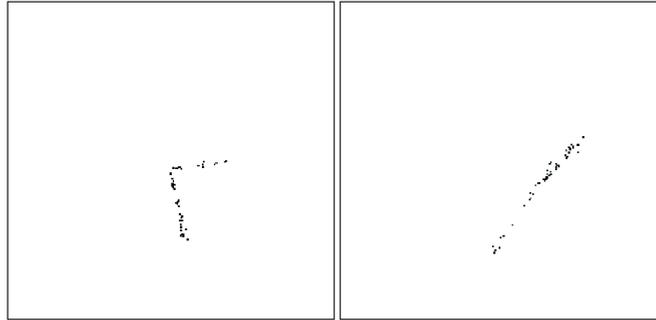
Three factors could explain the sudden death produced in the chip operating at these conditions:

- Applying -130 volts to the lower grid makes that the lower region is operated with a small gain. In this condition the charge entering from the upper region is amplified in the lower region. Finally in the lower region the same amount of electrons and ions that could be produced in a normal single stage InGrid will be produced in the lower region; this will lead to sparks

in the same way as in single stage devices.

- In a multiple GEM stack, where the distance between bottom GEM and readout chip is about 1 mm the field facing the chip is about 1 kV/cm. Our TwinGrid device presents a higher electric field (about 20 kV/cm) facing the chip surface.
- In the multiple GEM stack the charge diffuses in the 1 mm length extraction gap and in the gaps between GEMs. This way the amount of charge entering every pixel is reduced. If the chip is damaged because an excess of charge entering the pixels, in future TwinGrid designs the charge should be spread using a lower region of more than 50  $\mu\text{m}$  gap.

To continue measurements with a TwinGrid structure a new device was built on a Timepix chip. This chip was protected with a 11  $\mu\text{m}$  thick SiRN layer.  $^{55}\text{Fe}$  events and tracks from cosmic rays and electrons emitted by a  $^{90}\text{Sr}$  source were observed when operating the device at -200 V on the lower grid and -620 V on the upper grid. Cosmic rays were detected too when operating the device at -100 V on the lower grid and -540 V on the upper grid. Two typical examples of cosmic tracks are shown in figure 6.6.

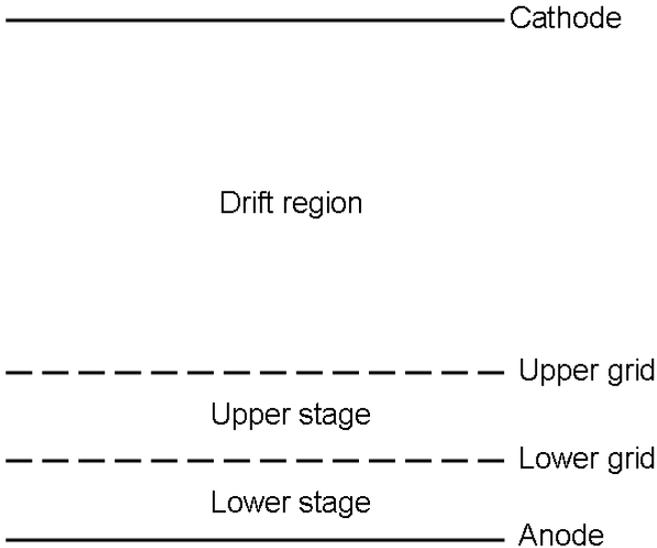


**Figure 6.6:** Two typical examples of cosmic rays tracks detected with a Timepix chip equipped with a TwinGrid structure. The Timepix chip was protected with a 11  $\mu\text{m}$  thick SiRN layer.

We conclude that the TwinGrid detector is fully functional, but still requires a special measure such as a spark protection layer to avoid sudden death.

## 6.4 TwinGrid gain and energy resolution

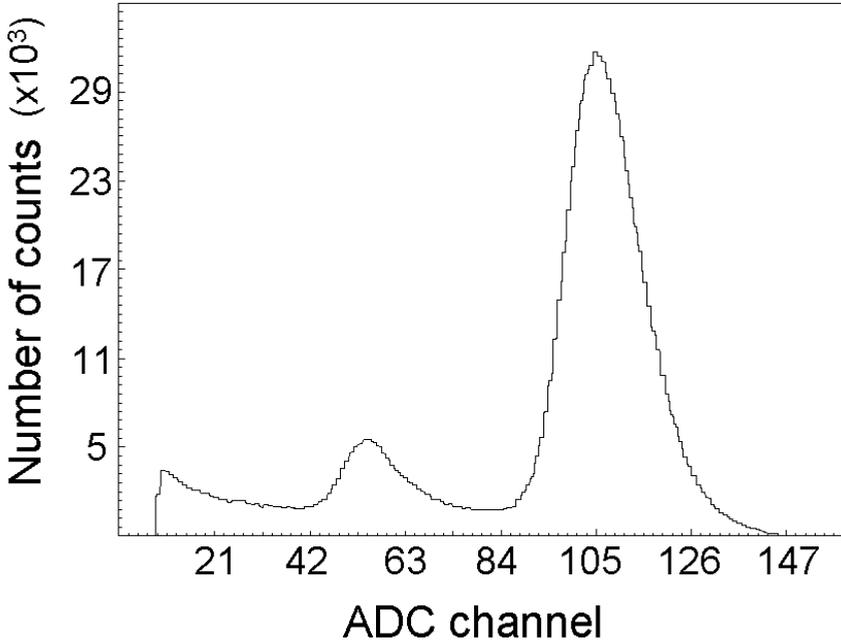
The gas gain and the energy resolution of TwinGrid (InGrid on top of GEM-Grid) were studied using structures built on dummy silicon substrates with an aluminized anode. The induced signals at the anode are amplified using a charge-sensitive amplifier. The output of the amplifier is connected to a multi-channel-analyzer from Amptek [120] to display and analyze the signals. The setup was the same one used for the characterization of the InGrid devices [62],[99]. An Ar/*i*C<sub>4</sub>H<sub>10</sub> (95/5) gas mixture was used for these measurements. A schematic of the different electrodes and regions in a TwinGrid detector is shown in figure 6.7.



**Figure 6.7:** Schematic picture of the different electrodes and regions in a TwinGrid detector.

From the <sup>55</sup>Fe spectrum recorded with the multi-channel-analyzer, the gain and the energy resolution can be extracted. A typical <sup>55</sup>Fe spectrum is shown in figure 6.8. The total gain of the system can be controlled by the voltages applied to the upper and lower grid.

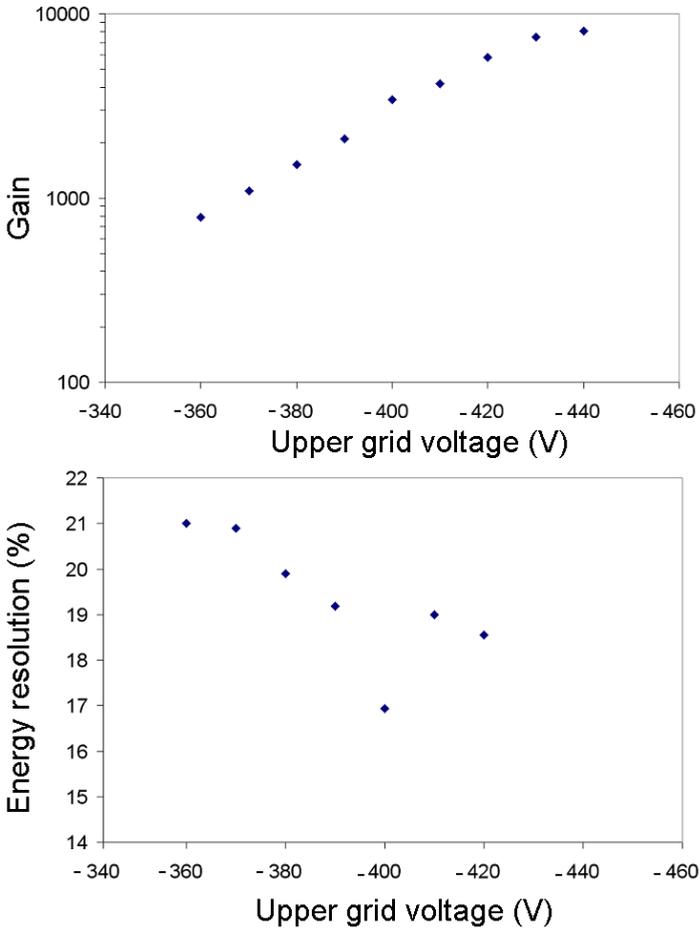
At first, the device was operated in the GEM mode. The lower grid is kept at a constant value of -50 volts and maintaining the drift field constant, the upper grid voltage was increased. In this configuration all the amplification takes place



**Figure 6.8:** Typical  $^{55}\text{Fe}$  spectrum displayed by the multi-channel-analyzer obtained with a TwinGrid device operated in a Ar/ $i\text{C}_4\text{H}_{10}$  (95/5) gas mixture. The applied voltages were  $V_{\text{upper grid}} = -410$  volts,  $V_{\text{lower grid}} = -50$  volts.

in the upper stage. This is considered to be the safest mode to avoid the risk of sparks. Figure 6.9 shows the gain curve and energy resolution plots measured with TwinGrid. A gas gain of several thousands and energy resolution of about 17% FWHM has been achieved. The best energy resolution is obtained at a gain of about 4000. A similar effect has been previously observed for Micromegas detectors [20]. TwinGrid does not produce a severe reduction in the performance in terms of gain and energy resolution when compared with InGrid. The performance of a standard single GEM [121] is improved when using a TwinGrid structure. The amount of insulator in a TwinGrid structure is less than in a standard GEM. Less insulator in the structure reduces charging up effects. This leads to a more uniform electric field and a reduced spark probability.

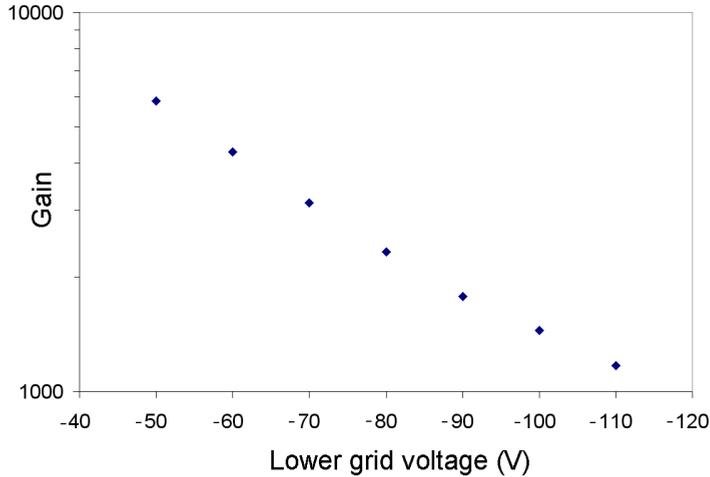
More measurements were done to confirm the correct behavior of the device.



**Figure 6.9:** TwinGrid gain and energy resolution plots in Ar/ $i$ C<sub>4</sub>H<sub>10</sub> (95/5). Drift field is kept at 1.2 kV/cm and -50 volts is applied to the lower grid.

The upper grid voltage and the drift field were kept constant while the lower grid voltage was increased. This configuration should reduce the field in the upper region, so a decrease in the gain is observed in figure 6.10. For voltages at which gain is expected in the lower region, the decrease of the gain in the upper region

compensates this effect. Therefore no increase in the gain is observed, rather, the gain decreases less rapidly with the lower grid voltage.

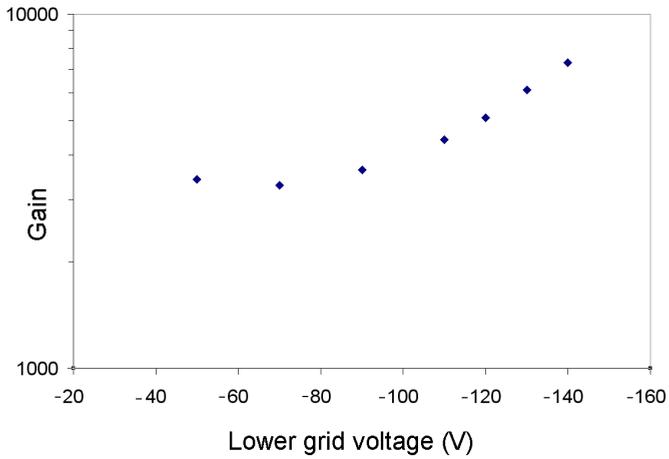


**Figure 6.10:** TwinGrid gain curve in Ar/ $i\text{C}_4\text{H}_{10}$  (95/5). Drift field is kept at 1.2 kV/cm and -420 volts is applied to the upper grid.

The gain of the device can be distributed between upper stage and lower stage. To test this property the device was operated with the field in the upper region and the drift field kept at constant values of 80 kV/cm and 1.2 kV/cm respectively. The lower grid voltage is increased. Figure 6.11 shows the obtained gain curve. The total gain of the device maintains a constant value until a certain lower grid voltage when amplification in the lower stage starts to happen. At this voltage the total gain of the device is the product of the upper stage (kept at a constant value) and the lower stage (that now is higher than one). A high gain is achieved with a very small gain in the lower stage.

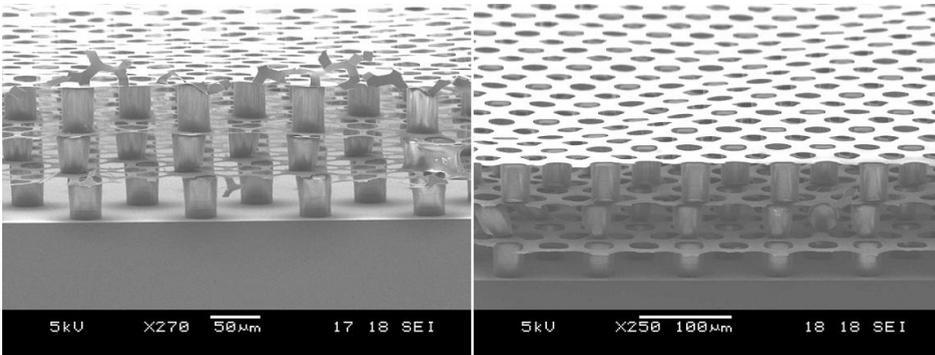
## 6.5 Three layer structures

Other designs of multilayer structures have been considered. A three layer stack can be produced following the fabrication process described at the beginning of this chapter with liquid SU-8. Figure 6.12 shows two of such structures with different design dimensions. These arrangements allow for effective gating



**Figure 6.11:** TwinGrid gain curve in  $\text{Ar}/i\text{C}_4\text{H}_{10}$  (95/5). Drift field is kept at 1.2 kV/cm and the upper region field is kept at 80 kV/cm.

to further reduce the ion poisoning in the drift region. Also the gain can be distributed along the three stages having more freedom in the high voltages applied.



**Figure 6.12:** SEM pictures of two different designs of triple grid structures.

These structures were not tested under high voltage conditions and radiation but the successful realization of the devices opens new possibilities for further

designs.

## 6.6 Conclusions

We have shown that TwinGrid devices are fully functional. Tracks of cosmic rays were recorded. Gas gains up to several thousands can be achieved.

The main goal of TwinGrid, chip protection against sparks, was not achieved. A chip equipped with TwinGrid without additional spark protection was destroyed. More spark tests must be done to determine if the intensity of discharges is reduced. The typical field applied to the lower region was about 20 kV/cm. More spark tests should be done having lower region fields of the order of 1 kV/cm. As in the GEM case it must be investigated which is the ideal lower stage thickness to eliminate sparks.



# Chapter 7

## Mechanical integrity of post-processed detectors

This chapter is devoted to the several issues that can affect the mechanical integrity of post-processed detectors [122]. The adhesion strength of SU-8 on different materials and its degradation under humidity conditions has been studied. The recently introduced negative photoresist KMPR [40] is evaluated as a replacement material for SU-8.

Finally the robustness of the detectors under mechanical impacts is studied. The ability of InGrid and GEMGrid devices to survive those impacts is compared.

### 7.1 Introduction

In previous chapters we have presented the performance of several radiation imaging detectors fabricated by CMOS compatible low temperature wafer post-processing. Prototypes fabricated with SU-8 as structural support, show excellent radiation imaging performance.

Devices are typically operated inside a sealed chamber or with a continuous gas flow of a mixture like He/ $i$ C<sub>4</sub>H<sub>10</sub> or Ar/ $i$ C<sub>4</sub>H<sub>10</sub>. Still, humidity is a functional hazard for these microsystems, as the devices are unpackaged. During storage and transport, humidity can affect the supporting photoresist pillars, leading to reduced flatness of the metal grid or even pillar detachment from the substrate. Clearly the detector functionality is then at stake.

In this chapter we compare the structural integrity of microsystems using both SU-8 and KMPR support structures after high-humidity bakes. The photoresists are tested on a variety of underlying thin films: PECVD  $\text{Si}_x\text{N}_y$  (200 nm), LPCVD a-Si:H (500 nm), or pure aluminum (1  $\mu\text{m}$ ). These materials are chosen because of their presence at the chip surface of the radiation imaging system [123].

Another factor that can affect the performance of the detectors is the mechanical integrity of the grid; being a 1  $\mu\text{m}$  thick metal layer, it is subjected to damage under mechanical attacks. The possible damage must be assessed to understand which critical steps during the fabrication process or storage and transportation must be specially addressed.

## 7.2 Materials and processing details

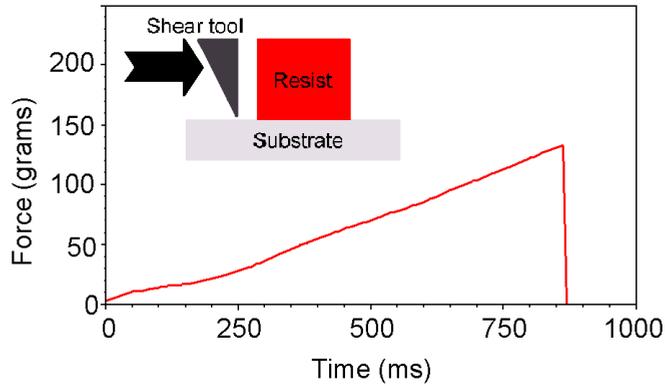
Silicon wafers, 4 inch size and 10  $\Omega\text{cm}$  resistivity were coated with SU-8 or KMPR. Prior to the photoresist spin coating, the substrates were cleaned in fuming nitric acid for 10 minutes. If the substrates were not coated with any metal a cleaning in hot nitric acid during another 10 minutes was performed and a short HF dip was realized to remove the native oxide. Just before spin coating the photoresist, a 10 minutes long dry baking at 120  $^\circ\text{C}$  was done.

The typical fabrication process for the detectors using SU-8 as structural material has already been described in chapter 3. As an alternative for SU-8 we also considered KMPR, a negative tone photoresist easily stripable, making it more suitable than SU-8 for electroplating molding [124]. The processing time for KMPR is shorter than SU-8 and it exhibits less internal stress. The maximum thickness of 100  $\mu\text{m}$  that can be obtained in a single spin coating process covers the range of interest for our system. The entire KMPR processing can be completed in one day following the standard procedure [40]:

- KMPR spin coat.
- Soft bake of the resist (15 minutes at 100  $^\circ\text{C}$ ).
- Exposure of the resist (80 seconds at 12  $\text{mW}/\text{cm}^2$ , near UV broad band 350 nm - 450 nm).
- Post exposure bake of the resist (4 minutes at 100  $^\circ\text{C}$ ).

## 7.3 Adhesion results

The adhesion of the SU-8 [46] and KMPR to the underlying layer was tested using a Dage 4000 shear tool [125]. The shear machine increases the force linearly until structures delaminate from the substrate or the machine force limit is reached. A typical force-time plot produced by the shear machine is shown in figure 7.1. In final detectors,  $30\ \mu\text{m}$  diameter pillars support the metal grid, but these pillars offered too small resistance against the shear test. For that reason test structures were fabricated consisting of SU-8 or KMPR squares with  $450\ \mu\text{m}$  side (unless stated otherwise) and  $55\ \mu\text{m}$  height.

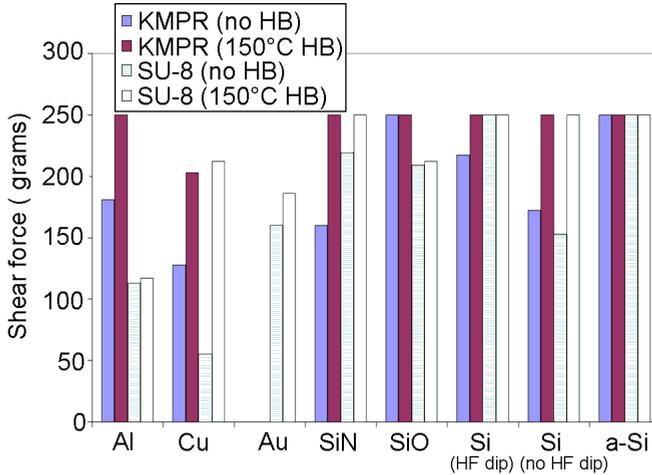


**Figure 7.1:** Typical force vs time plot produced by the Dage 4000 shear tool. The force is increased until the sample delaminates from the substrate, in this case at a force of about 130 grams.

### 7.3.1 Adhesion strength

First, the adhesion strength of SU-8 and KMPR over several underlying thin films was studied. The underlying materials were chosen either because they are present at the surface of a CMOS chip (silicon nitride, aluminum), or because they were considered to be added in the microsystem. Figure 7.2 shows the force needed to delaminate or break the tests structures from different substrates. Earlier work by Palacio et al. shows delamination of SU-8 under forces with the same order of magnitude (be it under different experimental circumstances) [126].

The figure shows that generally, KMPR shows better adhesion than SU-8. For both SU-8 and KMPR we find that specific details of the processing (soft bake, hard bake, etc.) have a considerable impact on the adhesion strength.



**Figure 7.2:** Adhesion force of SU-8 and KMPR on different substrate materials before and after a 150 °C hard bake. The force limit of the shear tool is 250 grams.

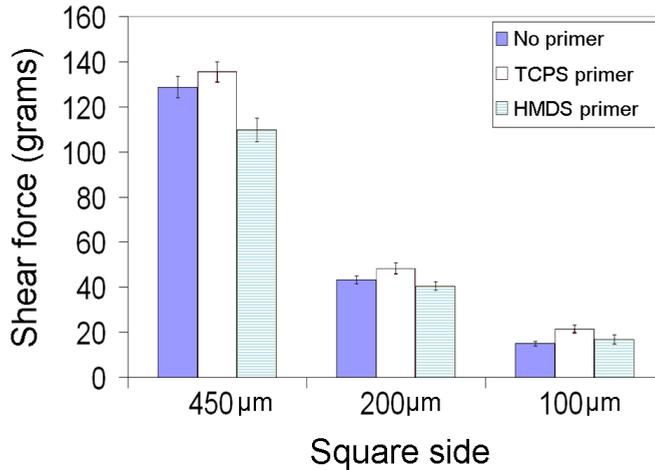
In all cases the SU-8 structures show delamination at the interface; KMPR structures on the other hand in several occasions break rather than delaminate. All silicon-based materials, which have a  $\text{SiO}_2$  native oxide, show good adhesion, and much better than the investigated metals. In all cases a 150 °C hard bake increases the adhesion considerably for both SU-8 and KMPR.

### 7.3.2 Primer treatment

As the SU-8 adhesion on metals was relatively poor in the above mentioned experiment, an additional experiment was conducted with this photoresist. In standard semiconductor manufacturing, prior to photoresist coating the substrate surface is coated with a thin primer layer to increase the resist adhesion [127]. Two primers commonly used are trichlorophenylsilane (TCPS) and hexamethyldisilazane (HMDS). The adhesion experiments were repeated using both primers, to investigate if the bond strength could be improved.

For the aluminum covered wafers, in the case of TCPS, samples were first cleaned with oxygen plasma. Then the TCPS vapor primer was applied and baked at 200 °C during 30 minutes. For HMDS priming, samples were cleaned in fuming nitric acid, the HMDS vapor primer was applied, without baking step. Finally SU-8 was spin coated on either primer following the typical fabrication process.

Figure 7.3 shows the results of the adhesion of SU-8 on an aluminum substrate for different square test structures with dimensions of 450  $\mu\text{m}$ , 200  $\mu\text{m}$  and 100  $\mu\text{m}$  side. Only small differences are observed: the adhesion is marginally increased with TCPS primer. HMDS primer has no effect.



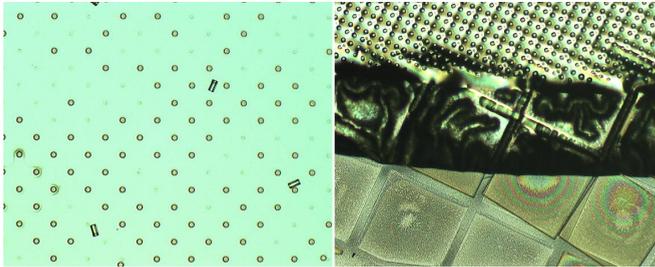
**Figure 7.3:** Adhesion of SU-8 on aluminum substrate for different primer treatments and different square sizes.

The shear force does not increase proportionally with the test structure area, but it is almost proportional to the side length. This proportionality is consistent with the observation that SU-8 releases through (progressive) delamination from the surface.

### 7.3.3 Exposure to humidity

Shear tests were also performed in samples exposed to humidity. The reduction of the adhesion strength under exposure to a high relative humidity (95% relative

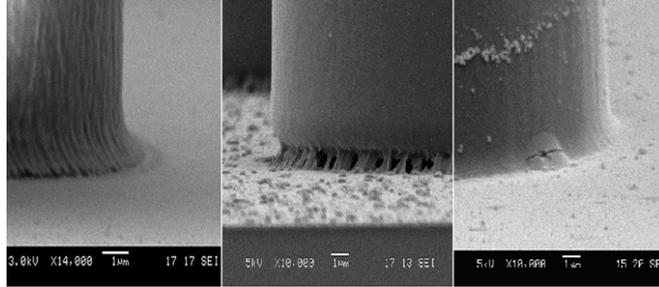
humidity at 30 °C unless otherwise stated) was studied for KMPR and SU-8 samples. SU-8 on aluminum shows a 50% reduction in adhesion strength after only one day, further decreasing to  $\sim 5\%$  of its original value after 3 weeks of exposure. In some samples adhesion was completely lost and the top grid or the pillars even peeled off during transportation. Figure 7.4 shows an optical microscope image of a device after moisture exposure. Several pillars can be seen detached from the substrate in figure 7.4 left. In figure 7.4 right it is seen how the grid became rough at the edge of the device, and even some of the support structures have moved or peeled off. This is a serious threat for the performance of the device as energy resolution will degrade with a rough mesh or the device even will stop working.



**Figure 7.4:** Optical microscope images of moisture exposed devices. Right: Rough grid at the edge of the detector, some support blocks have moved. Left: partially detached pillars and totally removed grid.

SEM inspection reveals the cause of the adhesion reduction. Figure 7.5 left shows a SU-8 pillar not exposed to humidity treatment; when compared with a SU-8 sample exposed to humidity, as in figure 7.5 center, it is seen that the SU-8 pillars have swollen evenly as much as 5% after the humidity treatment, likely by water absorption [128], [129]. At the interface between substrate and photoresist the swelling is less pronounced as the resist cannot expand freely. The SU-8 seems to detach from the aluminum interface (at least at the outside of the pillar), as shown in figure 7.5 (middle). Only some threads keep the pillar in contact with the substrate. On  $\text{Si}_x\text{N}_y$  or Si, the adhesion of SU-8 is better; but the swelling is the same, causing a dramatic reduction in the adhesion already after 1 or 3 days. This trend is shown in figure 7.6.

KMPR samples exposed to a few days of high humidity show a less dramatic reduction in the adhesion (figure 7.6). There even seems to be a slight improve-



**Figure 7.5:** SEM picture of SU-8 and KMPR pillars. Left: SU-8 pillar before exposure to humidity. Middle: SU-8 pillar after exposure to humidity. Right: KMPR pillar after exposure to humidity.

ment in the adhesion after 3 days exposure compared to the initial decrease after one day. This could be associated to a change in the material properties; it was observed that after three days humidity exposure the photoresist became more elastic and the shear tool deformed the resist test structure before delaminating it. However, it must be added that the quantitative results of identically treated samples vary with about 10% from wafer to wafer, so the difference between 1-day and 3-day adhesion is not very significant.

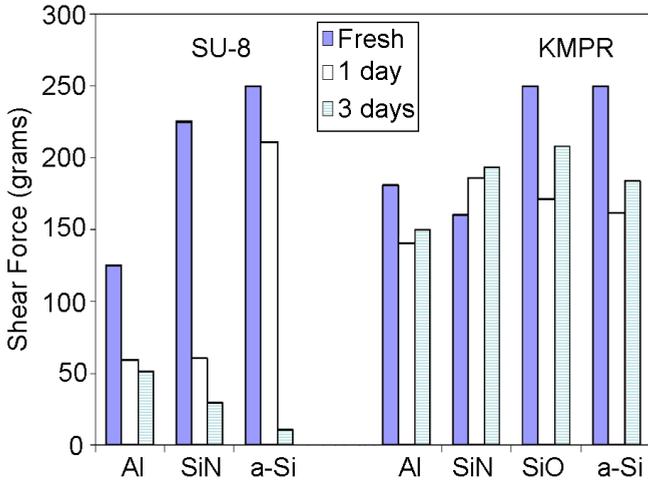
The SEM picture of a humidity exposed KMPR sample (figure 7.5, right) shows a good contact between substrate and photoresist. The threads that appeared in the SU-8 case are not present in the KMPR samples. KMPR shows a better interface between photoresist and substrate than SU-8, which leads to a better KMPR adhesion.

To confirm the difference in moisture response between SU-8 and KMPR longer humidity exposure times were studied as well as other substrate materials.

Figure 7.7 shows that even after 15 days of exposure to 95% relative humidity the KMPR samples on aluminum substrate maintain the original adhesion strength.

For the SU-8 samples the same adhesion reduction trend is found when the substrate is aluminum or a material with originally better adhesion, such as a-Si. It is concluded that adhesion loss is determined by the photoresist itself and not the substrate material.

The 95% relative humidity conditions are the most aggressive for the photoresists. It was observed that when samples are exposed to 75% or 85% relative



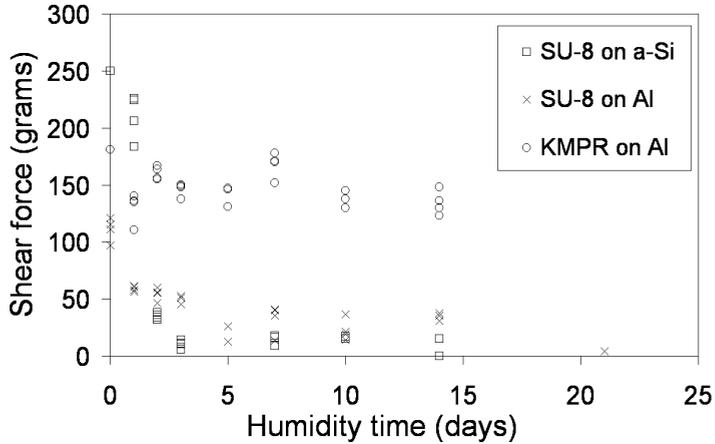
**Figure 7.6:** Adhesion strength of SU-8 and KMPR on different substrate materials; before humidity exposure (fresh) and after exposure to 95% relative humidity during one or three days.

humidity also at 30 °C the adhesion reduces at a lower rate. Figure 7.8 shows a comparison between the three different humidity conditions for SU-8 on aluminum. After 21 days at 75% relative humidity adhesion is reduced to about one third of its original value. Unexpectedly adhesion is apparently reduced at a faster rate for 75% relative humidity than for 85% relative humidity. With the given sample-to-sample variation ( $\sim 10\%$ ) this may be insignificant.

A functional test was performed with an InGrid device having SU-8 pillars, that was exposed to two weeks moisture conditions. After flushing the test chamber with an He/ $iC_4H_{10}$  (80/20) gas mixture, the leakage current between the grid and the anode became too high at -250 volts. At this voltage, no significant electron multiplication occurs yet. In other words, the microsystem failed the functional test after exposure to humidity.

### 7.3.4 Thermal cycling

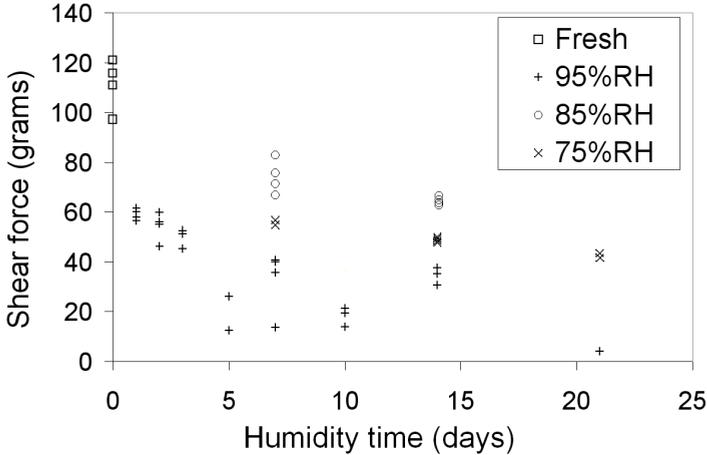
Several InGrid devices were also exposed to thermal cycling. All samples were cycled between 30 °C 95% RH and 0 °C for one day. The dwell time at high and low conditions was one hour and the ramp-up and ramp-down speeds



**Figure 7.7:** Adhesion strength of SU-8 over an aluminum substrate, a-Si substrate and KMPR over aluminum substrate when exposed to 95% relative humidity during several days.

were  $3\text{ }^{\circ}\text{C}/\text{min}$  and  $-1.6\text{ }^{\circ}\text{C}/\text{min}$ , respectively. The cooling down causes water condensation that might lead to corrosion of the aluminum anode. In case of SU-8 on aluminum indeed the adhesion strength was strongly reduced to 6 grams in shear force test compared to 125 grams for a fresh sample and 59 grams after 1 day at  $30\text{ }^{\circ}\text{C}$  and 95% RH. SEM inspection however did not show obvious signs of corrosion.

For SU-8 on other materials as well as for the KMPR samples a slightly better result was obtained after the cycling test than for a continuous exposure at  $30\text{ }^{\circ}\text{C}$ . This is in line with the shorter exposure time at the highest humidity condition. The samples with SU-8 test structures on aluminum and a-Si were cycled a second day between  $30\text{ }^{\circ}\text{C}$  at 95% RH and  $-10\text{ }^{\circ}\text{C}$ . It was expected that after condensation, water creeps into cracks or voids and expands when frozen; this could speed up the degradation. For the standard sample with SU-8 test structures on aluminum the degradation after the first day is already so large that the impact of freezing the detector does not cause a measurable decrease in adhesion strength. For the SU-8 test structures on the silicon substrate, the degradation is not larger than could be expected after two days exposure at high humidity.



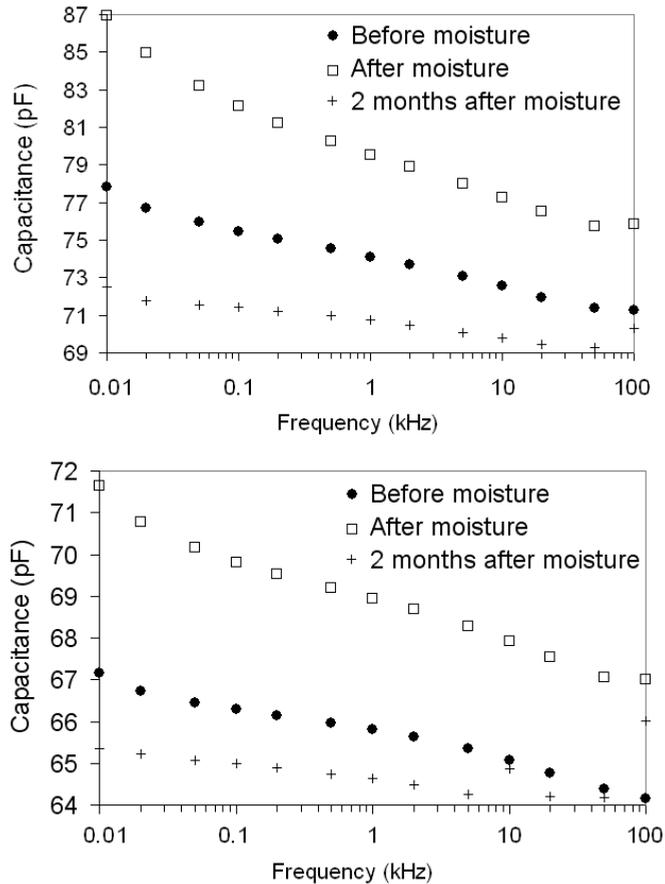
**Figure 7.8:** Adhesion strength of SU-8 over an aluminum substrate when exposed to different relative humidity percentages at the same temperature of 30 °C during several days.

## 7.4 Electrical tests

The effect of the moisture exposure has also been studied by capacitance-voltage measurements. Due to moisture, SU-8 supporting pillars may swell leading to a change in area and height. Also the absorbed moisture might change the pillar relative permittivity. These two effects should be reflected in a capacitance change of the devices before and after humidity exposure.

The small-signal capacitance at 0 volts and different frequencies was measured with a Cascade Microtech 11000 Probe Station for two kind of InGrid devices; named field number 9 and field number 11, both having an area of about 1200 mm<sup>2</sup>. Design parameters for those devices are shown in table 7.1. An increase in the capacitance of about 4 pF for field 11 (bottom) and 6 pF for field 9 (top) is observed after a moisture exposure of 3 days. The capacitance variation is due to the change in the height and area of the pillars and the increase in the relative permittivity because of the water absorption. Figure 7.9 shows the change in capacitance for fields 9 and 11 after the humidity exposure. It is observed that after two months of normal ambient conditions the capacitance is slightly lower than its original value; consistent with the expected diffusion of humidity out

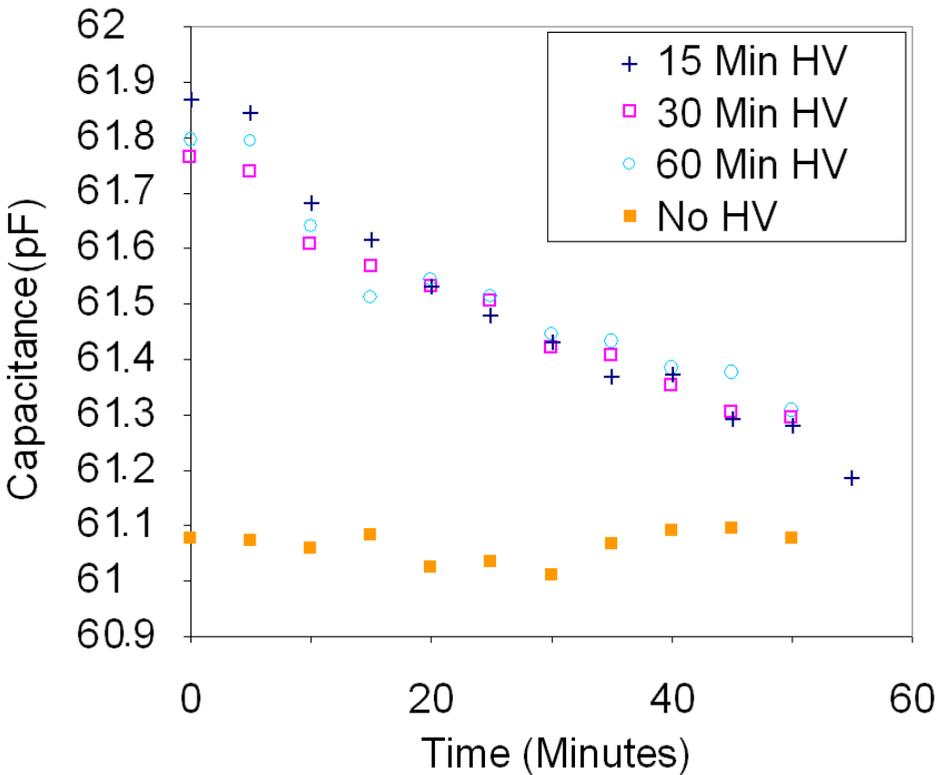
from the SU-8 [129] and the change of height and diameter in the SU-8 pillars. Even if the capacitance is restored to its original value, moisture is still a problem as adhesion strength will not be recovered and pillars can be already detached from the substrate.



**Figure 7.9:** Capacitance measurements before exposure to humidity, directly after exposure to humidity and two months after the humidity exposure in two different InGrid devices (top: field 9, bottom: field 11) at different frequencies.

The capacitance of InGrid devices was also measured after high voltage stress.

For that purpose, 400 volts were applied to the grid during 15 minutes, 30 minutes and 60 minutes. A small increase in the capacitance is observed after this stress and it slowly goes down to the original value before the high voltage conditions. This same experiment was performed in Metal-Insulator-Metal capacitors (being SU-8 the insulator layer and aluminum the metal layers) and the capacitance change effect was not found. This rules out a charging up or deformation of the SU-8 as root cause of the capacitance change. A relaxation effect in the metal grid is a possible explanation for the capacitance change. Figure 7.10 shows the capacitance change after exposure to high voltage conditions.



**Figure 7.10:** Capacitance change of an InGrid device before and after different times of high voltage stress as a function of time.

## 7.5 Mechanical stability

The mechanical stability of the thin metal foil was studied analyzing the mechanical displacement of the grid at high frequency, performing mechanical attacks and wind tests. Two different InGrid designs were fabricated, named design 4 and design 7, with different pillar pitch, hole pitch and hole diameter. Table 7.1 shows the design parameters for those fields.

design number	hole diameter	pillar diameter	hole pitch	pillar pitch
field 4	11 $\mu\text{m}$	30 $\mu\text{m}$	32 $\mu\text{m}$	128 $\mu\text{m}$
field 7	15 $\mu\text{m}$	30 $\mu\text{m}$	45 $\mu\text{m}$	90 $\mu\text{m}$
field 9	30 $\mu\text{m}$	30 $\mu\text{m}$	45 $\mu\text{m}$	90 $\mu\text{m}$
field 11	29 $\mu\text{m}$	30 $\mu\text{m}$	58 $\mu\text{m}$	116 $\mu\text{m}$

**Table 7.1:** Design parameters for four different InGrid devices used in the reliability tests.

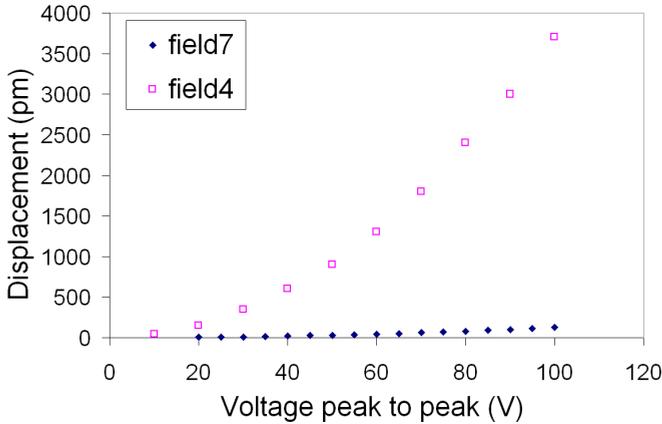
### 7.5.1 Mechanical deflection

Due to the electro-static force some deflection of the InGrid membrane is expected between pillars when the high voltage is applied. In typical MEMS systems the deflection can be measured by the change of capacitance due to the mechanical deformation [47]. This technique cannot be applied in our case, as the pillar height is in the order of 50  $\mu\text{m}$  the grid displacement induced by the electro-static force will produce a minimal change in the capacitance.

To overcome this problem an alternative measurement technique based on light interference was used. A MSA-500 vibrometer from Polytec [61] was used to measure the deflection of the membrane. The resolution of the equipment in optimal conditions is in the order of 10 picometers, so very small deflections can be detected.

For the measurements the membrane was excited with a 100 kHz sinusoidal wave and a maximum peak to peak voltage of 100 volts. Figure 7.11 shows the displacement as a function of the applied voltage for fields 4 and 7. Maximum displacement for field 4 is in the order of 4 nm, and 125 pm for field 7. This displacement will not change significantly the amplification gap of the device, that defines the gain for a given voltage.

Simulations were done using COMSOL finite element modelling software. The resonance frequency for the system is in the MHz range. This kind of frequencies



**Figure 7.11:** Maximum grid displacement for two different InGrid devices when applying a 100 kHz frequency signal.

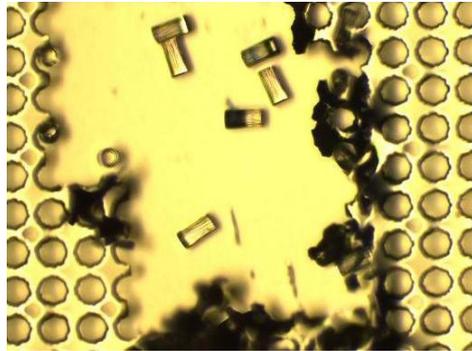
are never expected to be faced by the detector. As seen in figure 7.11 frequencies in the kHz range do not produce significant deformation in the grid. Therefore the mechanical stability of the grid is assured.

### 7.5.2 Ball point test

To compare the mechanical robustness of Micromegas-like and GEM-like structures, several devices were built on dummy silicon wafers and subjected to mechanical attacks. We investigated the ruggedness of the detectors when an object impacts on them. This test was inspired by the ball drop tests used in the liquid crystal display community [130] and the ball point pen drop test known from fingerprint sensors [131]. Our first test consists in dropping a ballpoint pen from a certain distance above the device to assess the damage.

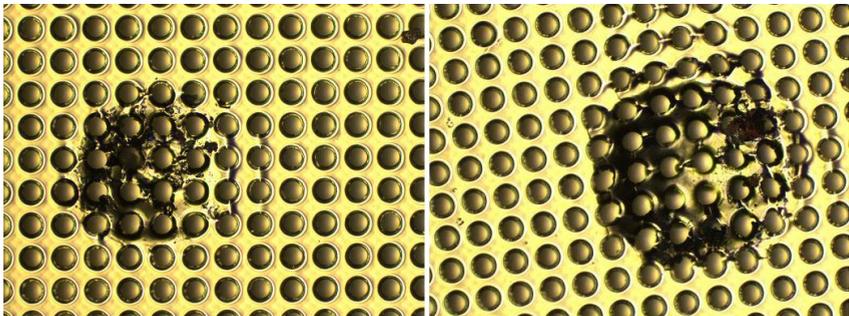
For the InGrid device, as seen in figure 7.12, just dropping the ball pen from a 1 cm distance can cause severe damage as the ball pen can scratch the grid after bouncing. As conducting as well as insulating material is detached from the detector surface, this damage can be assumed to disable the device.

For the GEMGrid the damage is less pronounced as the pen bounces on the device and does not scratch the grid. Instead, only an imprint of the tip of the ball pen is observed on the GEMGrid, as shown in figure 7.13. All material



**Figure 7.12:** Optical microscope image of an InGrid device after the drop test at 1 cm. A large scratch in the grid is produced and pillars are detached from the substrate.

seems to remain in place, even when a higher drop distance of 5 cm is employed. Comparing figures 7.12 and 7.13, the GEMGrid detector exhibits much better robustness against vertical mechanical attacks. Still, even in the GEMGrid case a ballpoint drop will adversely affect the detector functionality locally around the impact point.



**Figure 7.13:** Optical microscope image of a GEMGrid structure with recessed SU-8 after the drop test at 1 cm (left) and 5 cm (right).

The drop ball pen test caused serious damage to the InGrid. To investigate the

behavior under smaller forces, the tip of a Dektak profilometer from Veeco [132] was moved along the grid of both InGrid and GEMGrid. The maximum force that can be applied by the profilometer was 15 mg and no damage was observed for any device. In the InGrid case some mechanical displacement of the grid can be observed but it is restored to its original position once the force stops.

### 7.5.3 Wind test

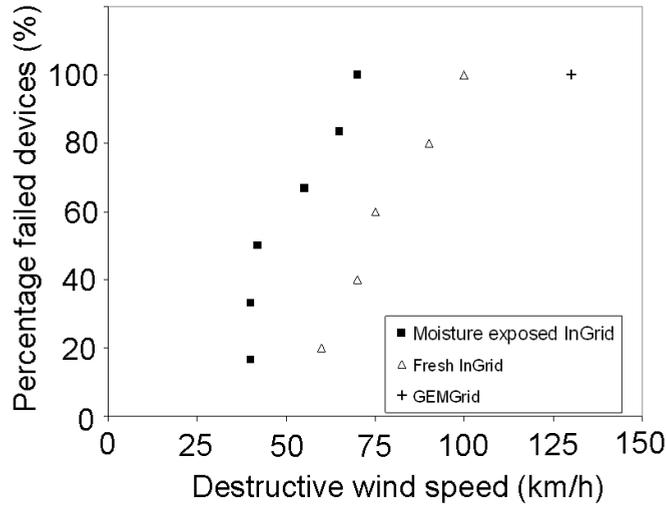
InGrid and GEMGrid devices were exposed to air flow to assess the resistance of the grid to high speed winds. The wind flow was generated from a compressed air gun with a 1.5 mm nozzle and measured with a pocket wind meter. The samples were placed at an angle of  $45^\circ$  with respect to the air flow. In both cases the metal grid peeled off from the SU-8 supporting structures but the SU-8 itself remained attached to the substrate. Samples previously exposed to moisture conditions were also tested under wind conditions. Figure 7.14 represents the distribution of the cumulative number of samples which grid peels off at a certain wind speed. This distribution is used to represent weakest link reliability data. Samples previously exposed to humidity is the first group to fail and at 70 km/h the grid has peeled off in all the samples. Even in the samples previously exposed to humidity SU-8 structures remained attached to the substrate. Comparing InGrid and GEMGrid a much earlier failure is produced in InGrid devices. All of them have failed at a speed 95 km/h while 130 km/h are needed to make the GEMGrid fail.

Such air flows are improbable in storage or detector operation conditions. However dry-nitrogen blow cleaners, commonly applied during microsystem manufacturing and assembly, could be operated in this regime. Hence, such instruments should be carefully used in the manufacturing of integrated grid structures, be it Micromegas-like or GEM-like.

## 7.6 Conclusions

To conclude this chapter we would like to summarize some recommendations for the storage and transportation of the devices.

- Detectors must be stored in a dry environment. Typically our devices are stored in a nitrogen chamber. The adhesion of the grid supporting structures degrade dramatically only after one day exposed to high humidity environments.



**Figure 7.14:** Distribution of the number of failed devices as a function of the wind speed for moisture exposed InGrid devices, fresh InGrid devices and one fresh GEMGrid device.

- As the devices are not packaged they are prone to be mechanically damaged. A temporary packaging is recommended, specially for InGrid devices.
- Mechanical vibrations during transportation of the detector are not in the range of the resonance frequency of the detector. No stability problems are foreseen in that sense.
- SU-8 shows better adhesion with a-Si or  $\text{Si}_x\text{N}_y$  than with metals. The use of high resistive layers as antispark layers also improves the robustness of the detector from the mechanical point of view.
- KMPR photoresist shows better adhesion than SU-8. Also the moisture resistance is better in the KMPR case. Devices using KMPR as structural support must be studied.



# Conclusions and future work

To finish this thesis the main research results are summarized in this chapter. We conclude giving remarks on still open issues for further investigation.

## 8.1 Conclusions

In this thesis we have shown that Micromegas-like and GEM-like detectors can be built using wafer post-processing technology. In a further step those detectors have been integrated on top of CMOS chips. The integrated devices show superior performance when compared with manually assembled detectors. Particle tracking with high single electron efficiency is possible.

Multistage detectors have been built on top of CMOS chips using wafer post-processing technology. The fabrication process is successful, but still at a low yield. These detectors open new possibilities to study spark problems and signal development.

A fair comparison between Micromegas-like and GEM-like structures made with the same materials and same geometry can be done. GEM-like structures with non-recessed SU-8 present lower spark limit than the Micromegas-like structures. When GEM-like structures are built with recessed SU-8 the performance is similar to the Micromegas-like devices.

Micro Patterned Gaseous Detectors are prone to suffer spark problems. These discharges can destroy the readout electronics. We have shown that using a high resistive layer we can protect CMOS chips in an adequate way. SiRN and a-Si:H

can be used as anti-spark layers. Future gaseous detectors are not required not to spark.

As the detectors are unpackaged they can suffer several reliability issues. We studied how humidity and mechanical impacts can degrade the detectors. A guideline for its manufacturing is provided.

## 8.2 Future work and recommendations

Based on the work done in this thesis new questions and demands have arisen. We would like to remark some of the ideas that should be investigated and the work that must be done.

The fabrication of a grid made out of a high resistive material is a main goal. The charge spread produced by the actual spark protection layer would then be eliminated.

Thicker grids made by copper electroplating are within reach. This will overcome the problem of the relative fragile grids made out of aluminum.

A deeper study of the double layer structures must be done. Literature indicates the spark limit of this kind of detectors is higher than in single layer structures. The geometry needed to reproduce those results in our detectors must be investigated.

The signal development of the multistage detectors is of extreme interest. The signal at the pixels is mainly induced by electrons which should make the time response of the detector very fast.

All our experiments have been done using single chips. The tiling of several chips together to get bigger area detectors is expected to be done soon.

A new polymer, Durimide from Fujifilm has caught our attention. It has a high transition glass temperature. PECVD silicon nitride can be deposited on top of the material. More studies must be done using Durimide or similar polymers as structural material.

The replacement of SU-8 with ceramic materials is under study.

New beam tests will be done in the future using larger area detectors. A beam telescope positioning several detectors in line will be constructed. Measurements to determine the spatial resolution of the detectors must be realized.

The integration of InGrid or GEMGrid on new readout chips (PSI-46, GOS-SIPO) commonly used by the particle tracking community will be done in a near future. Although no technological challenge is foreseen the prototypes realization will prove further the concept.

Finally, the main challenge to compete with GEMs, Micromegas, or silicon

detectors is mass production. If InGrid or GEMGrid can be produced in full 8-inch wafers it will be possible to provide other institutes with devices to spread this technology faster.

The ultimate goal is to cover large areas with our detectors.



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# Summary

In this thesis several post-processing steps that have been applied to CMOS chips are presented. Gas amplification structures are built on top of the microchips. A complete radiation imaging gaseous detector is obtained this way. The purpose of the research presented in this thesis is to develop the technology needed to fabricate the previously mentioned radiation imaging detectors and determine its performance.

Integrated Micromegas-like and GEM-like structures were fabricated on top of Timepix CMOS chips. Single electron efficiency, measured by counting the number of detected electrons from an  $^{55}\text{Fe}$  conversion in  $\text{Ar}/i\text{C}_4\text{H}_{10}$  (95/5) was found to be well above 90%. The detector provides high single electron efficiency and three dimensional reconstruction of the trajectory of electrically charged particles. It has a fine pixel pitch and a low mass. All these features make it a suitable candidate for tracking of charged particles in future detectors like ATLAS or CMS after the LHC upgrade or the International Linear Collider.

Micromegas-like and GEM-like structures can be compared fairly as same materials and dimensions can be used. It was found that GEM-like structures having a large amount of insulator perform worse than similar Micromegas-like structures. The maximum achievable gain before sparks appear is lower for GEM-like than for Micromegas-like. When the amount of insulator is reduced in the GEM-like structures, having recessed insulator walls with respect to the metal electrodes, the performance is similar to Micromegas-like structures.

Multistage detectors on top of Timepix chips were also built using wafer post-processing. The devices were fully operational and cosmic rays could be detected. The spark rate of multistage detectors compared to single detectors must be studied further. Also the signal development in these detectors is expected to be

faster than in single stage detectors.

Spark damage is a common problem in gaseous detectors. Sparks can destroy the readout electronics. We have deposited a-Si:H and SiRN on Timepix chips. We have shown that these high resistive layers deposited on top of the CMOS chip can help to reduce the spark problems. Discharge energy is reduced and microchips can survive discharges that otherwise would destroy them. Future detectors no longer need to be spark-less as they can now be made spark proof.

Integrated detectors can suffer reliability problems because of degradation due to moisture exposure. Also mechanical attacks can prevent the devices from working. We have evaluated these problems to give storage and transportation recommendations. The use of other materials less sensitive to humidity was also studied.

# Samenvatting

Dit proefschrift toont verschillende technieken voor de nabehandeling van CMOS chips. De structuren die daarmee gemaakt kunnen worden dienen voor elektronen vermenigvuldiging in een gas omgeving. Op deze wijze is een beeldvormende detector gemaakt bovenop een daarvoor geschikte microchip.

Het doel van het onderzoek is het ontwikkelen van technieken om de boven genoemde detectoren te vervaardigen. De functionaliteit van de verschillende prototypes wordt daarna getest.

De op CMOS chips geïntegreerde structuren hebben ofwel een zogenaamde Micromegas- ofwel een GEM-architectuur. De efficiëntie voor detectie van individuele elektronen is meer dan 90%. Dit is bepaald door het tellen van gedetecteerde elektronen na de conversie van  $^{55}\text{Fe}$  fotonen in  $\text{Ar}/i\text{C}_4\text{H}_{10}$  (95/5). De detector beschikt over een hoge gevoeligheid voor losse, individuele elektronen, is geschikt voor driedimensionale reconstructie van het pad van geladen deeltjes en heeft een kleine pixel maat en een lage massa. Met deze eigenschappen is de detector geschikt voor het volgen van geladen deeltjes in toekomstige instrumenten zoals ATLAS en CMS (na de LHC upgrade) of voor de International Linear Collider.

De Micromegas en GEM architectuur kunnen eerlijk vergeleken worden zolang de materialen en geometrie die gebruikt worden vergelijkbaar is. De GEM-achtige structuren, met een relatief grote hoeveelheid diëlektricum, hebben een slechtere werking dan vergelijkbare structuren met een Micromegas-achtig ontwerp. De maximaal haalbare vermenigvuldigingsfactor voordat vonkvorming optreedt, is lager voor de GEM- dan voor de Micromegas-ontwerpen. Wanneer de hoeveelheid diëlektricum kleiner wordt, door de wanden smaller te maken ten opzichte van de metaal elektrode erbovenop, verbetert de werking tot het niveau van de

Micromegas-achtige structuren.

Het proefschrift doet tevens verslag van meertraps detectoren gemaakt met nabehandelingstechnieken bovenop CMOS chips, in dit geval Timepix. Deze instrumenten zijn volledig operationeel en in staat om kosmische straling te detecteren. Deze meertraps detectoren zijn bedoeld voor het verlagen van de frequentie van vonkvorming ten opzichte van de normale, enkelvoudige structuren. Daarnaast is de verwachting dat deze nieuwe detectoren in staat zijn tot snellere signaalforming. Verder onderzoek naar de effectiviteit op deze vlakken is nodig.

Schade door vonkvorming is een groot en bekend probleem voor gas-gevulde detectoren. De elektronica voor uitlezing van het signaal (in dit geval de chip) kan beschadigd worden door vonk erosie. Ter bescherming zijn lagen van a-Si:H (amorf silicium) en SiRN (Si-rijk siliciumnitride) aangebracht op het chip oppervlak. Deze lagen hebben een hoge vierpuntsweerstand en ze kunnen de beschadiging na vonkvorming verminderen. De hoeveelheid energie per ontlading is verlaagd en de microchips kunnen ontladingen doorstaan die anders destructief zouden zijn. Deze vonk-bestendige detectoren vereisen niet langer dat vonkvorming in de detectie kamer volledig uitgesloten is.

De betrouwbaarheid van geïntegreerde detectoren kan verslechterd worden door structurele veranderingen als gevolg van blootstelling aan een hoge relatieve vochtigheid. Ook mechanische invloeden kunnen een nadelig effect hebben. De genoemde problemen zijn onderzocht met het oog op het bepalen van de juiste handelwijzen tijdens opslag en transport. Ook is onderzoek verricht aan het gebruik van alternatieve materialen met een lagere gevoeligheid voor invloed van vocht.

# List of publications

V. M. Blanco Carballo, Y. Bilevych, M. Chefdeville, M. Fransen, H. van der Graaf, C. Salm, J. Schmitz and J. Timmermans. *TwinGrid: a wafer post-processed multistage Micro Patterned Gaseous Detector*. To be submitted to Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment.

V. M. Blanco Carballo, Y. Bilevych, M. Chefdeville, M. Fransen, H. van der Graaf, C. Salm, J. Schmitz and J. Timmermans. *GEMGrid: a wafer post-processed GEM-like radiation detector*. Submitted to Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment.

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